A CAHNERS PUBLICATION INTERNATIONAL EDITION APRIL 12, 1990

EDN®

SPECIAL ISSUE: Communications

MCA and EISA compete for board designs

Optimizing C compilers for single-chip µPs—Pt 2

EDN's All-Star PC—Pt 3

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Modem chip sets raise their standards

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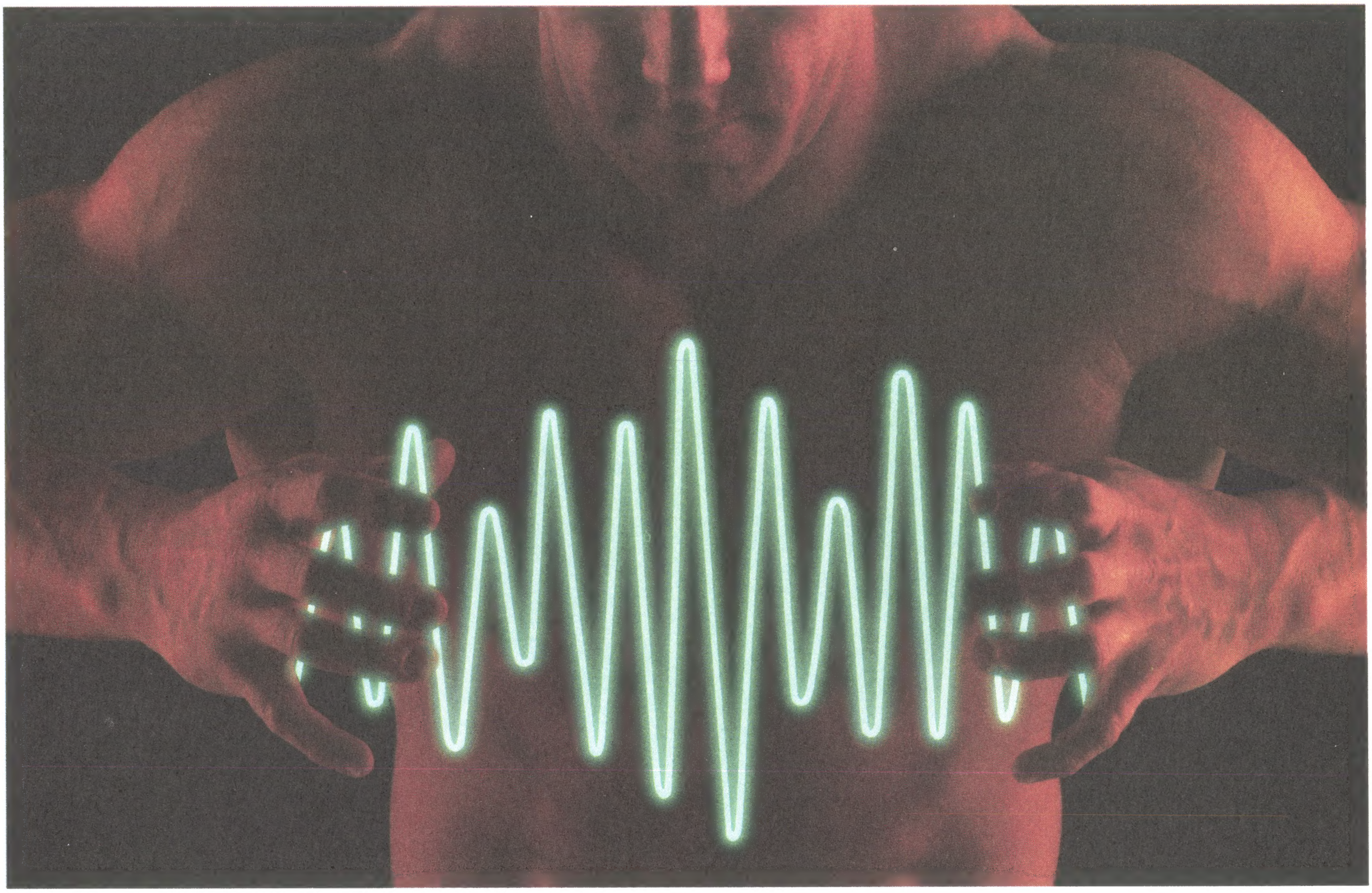

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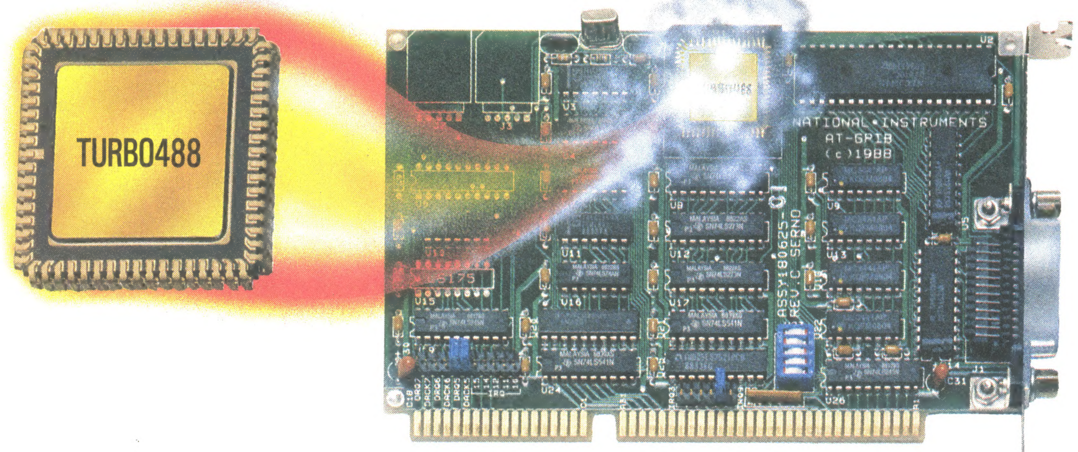

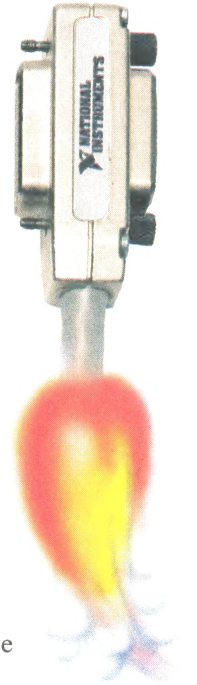

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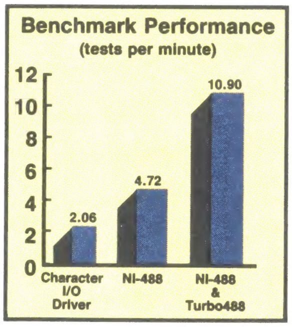

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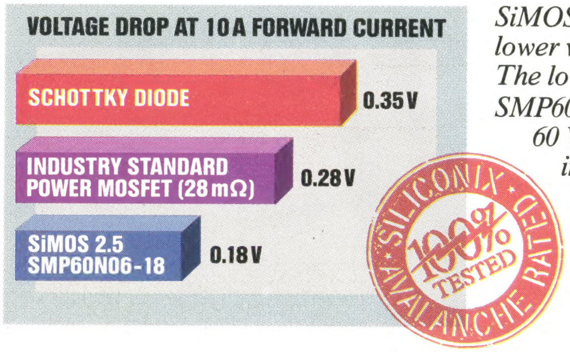

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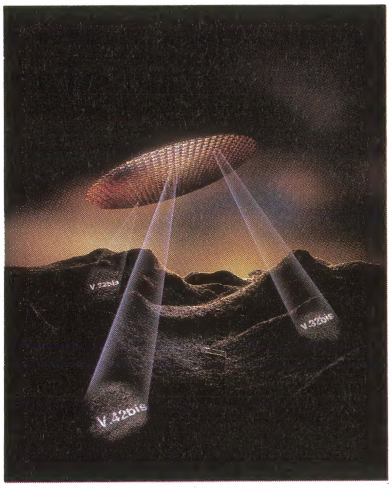
Volume 35, Number 8

April 12, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Advanced modem chip sets comply with the latest standards to make your communications quality soar. See the Special Report on pg 94. (Photo courtesy Rockwell International, art direction by Mike Lantow; photography by Richard Wahlstrom)*

COMMUNICATIONS SPECIAL ISSUE

SPECIAL REPORT

Modem chip sets 94

Modem chip sets now offer error-correction schemes and data-compression algorithms. They also use DSP to implement advances in modulation and coding techniques. These advances promise to make data- and fax-modem communications over the dial-up telephone network faster and more reliable than ever before. *—Maury Wright, Regional Editor*

EDN's All-Star PC Project—Part 3 117

INNOVATION™ Driving Electronic Technology Into The Next Century

Nothing in computer design depends more on fuzzy factors, such as touch, feel, or shade, than the PC's human interface. Yet no ingredients affect the PC's utility more. A few standards exist for defining such human-interface factors as keyboard angle, key layout, and screen contrast, but these standards establish an ideal environment for that mythical person: the Typical User.*—Steven H Leibson, Senior Regional Editor*

DESIGN FEATURES

Specific optimizations adapt C to single-chip μPs—Part 2 131

The first part of this 2-part series contrasted how conventional C programs should work and how well single-chip μPs suit C. This part covers C extensions and optimizations tailored for specific single-chip μPs and includes detailed programming tips for writing tight C programs.*—Charles H Small, Senior Editor*

Routing out signals troubleshoots LCA designs 151

Although you can use ASIC design-verification techniques, such as software simulation, with Xilinx LCA field-programmable gate arrays, these devices will also yield to traditional in-circuit methods.*—John Rostykus, Data I/O Corp*

Continued on page 7

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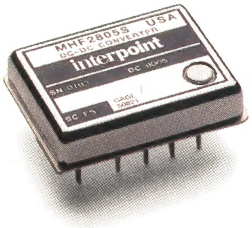

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EDN Magazine Edition®

April 12, 1990

Inexpensive 16-bit debugging tools *satisfy many application needs without busting your budget, albeit with less power than the more expensive tools (pg 77).*

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

Express Request

Create accurate analog models for better simulations 167

Even the best simulator provides bad results if you use poor models. Although most commercial analog simulators come with libraries of device models, these libraries often lack the complex models you need. As a result, you may have to build your own models.—*Eric S Filseth, Jeff Berwick, and Harold Mann, Valid Logic Systems*

TECHNOLOGY UPDATES

MCA and EISA square off 61

The proponents of the latest small-computer marketing conflict—those in favor of either the Micro Channel Architecture or the Extended Industry Standard Architecture—have taken hostages from the community of plug-in-board manufacturers. However, many board developers have declared this battle of the buses to be a win/win situation: They've hedged their bets by designing products for both bus specifications.—*J D Mosley, Regional Editor*

16-bit debugging tools perform at low cost 77

A favorite way for budget-conscious managers to control project costs is to disapprove the purchase of expensive (>$10,000) test equipment, such as processor-specific debugging tools. Lower-cost (<$6500) alternatives can satisfy many applications and may be the best choice for your tight budget—if you can live within their limitations.—*Richard A Quinnell, Regional Editor*

EDITORS' CHOICE

Comprehensive CAE and CAD package 86

PRODUCT UPDATES

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IBM VGA graphics controller 92

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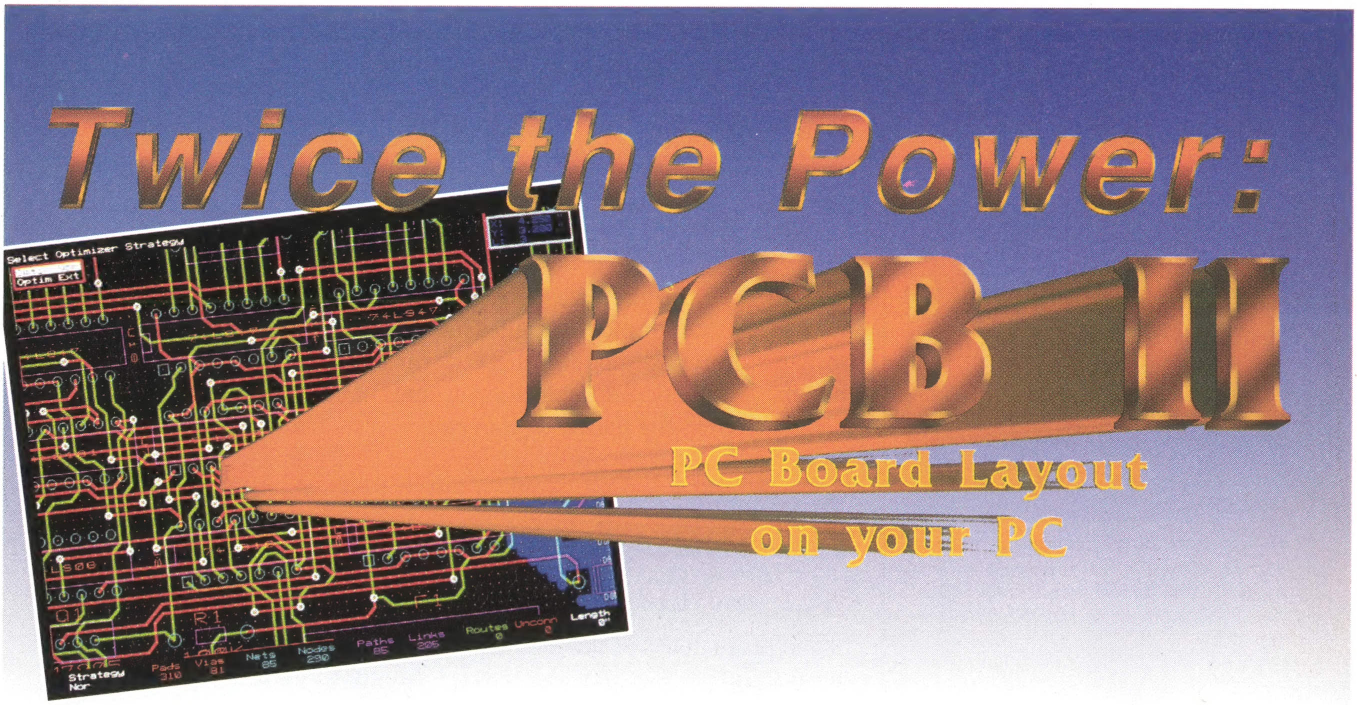

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Jonathan Titus
Managing Editor
Joan Morrow
Assistant Managing Editor
Susan L Rastellini
Special Projects
Gary Legg
Home Office Editorial Staff
275 Washington St, Newton, MA 02158
(617) 964-3030
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Brian Kerridge, *European Editor*
(603) 630782
(St Francis House, Queens Rd,
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EDITORIAL 55

The future of high-definition television (HDTV) depends on fiber optics, not on technology that jams a 30-MHz signal into a 6-MHz broadcast-TV channel.

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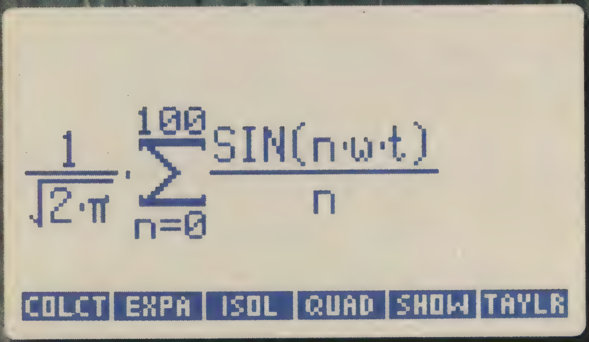

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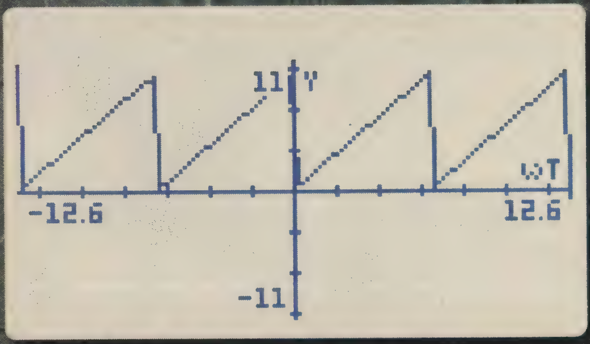

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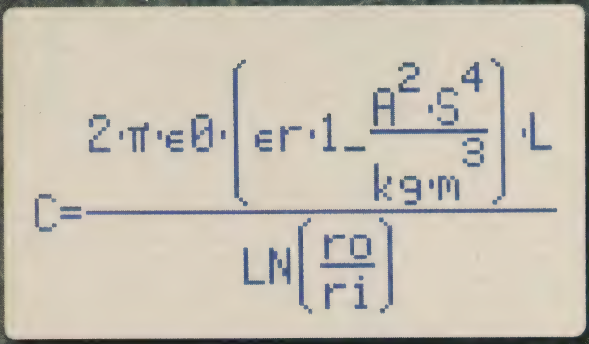

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AMD was part of setting the standards long before the Advanced Networking Group. (We've been on the ANSI standard committee since its inception.)

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CIRCLE NO. 31

INTRODUCI
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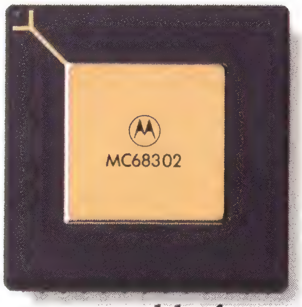

Quick, who was the last "great communicator?" Ah, well, it doesn't matter. Not even he controlled the world of communications as well as you can now.

And with a single chip, at that. Namely, Motorola's 68302 Integrated Multiprotocol Processor.

CONTROL ALL FORMS OF COMMUNICATIONS.

That's a big promise, but the 68302 is more than up to it. With three high performance serial communications controllers, each with multiprotocol capabilities, the 68302 can run anything from ISDN, WANs and packet networks to bridges, concentrators, gateways, peripheral I/O, modems and more.

ISDN, by the way, leads that list for a very good reason. Because the 68302's multiprotocol capabilities are the first sensible way to migrate today's proprietary and defacto protocols to emerging standards like ISDN.

RUN ON A POWERFUL 68000 PLATFORM.

The 68302 operates on a 68000-based core and it's fully compatible with the wide world of existing 68000 software. And with our growing 68300 family of microcontrollers.

All that compatibility, obviously, can save you loads of development time and lots of money.

In addition to the 68000-core processor, the 68302 features a powerful, high-speed RISC-based communications processor.

This dual processor approach yields efficient communications processing. Not to mention the highest performance communications controller on the market.

Winner 1988
Malcolm Baldrige
National
Quality
Award

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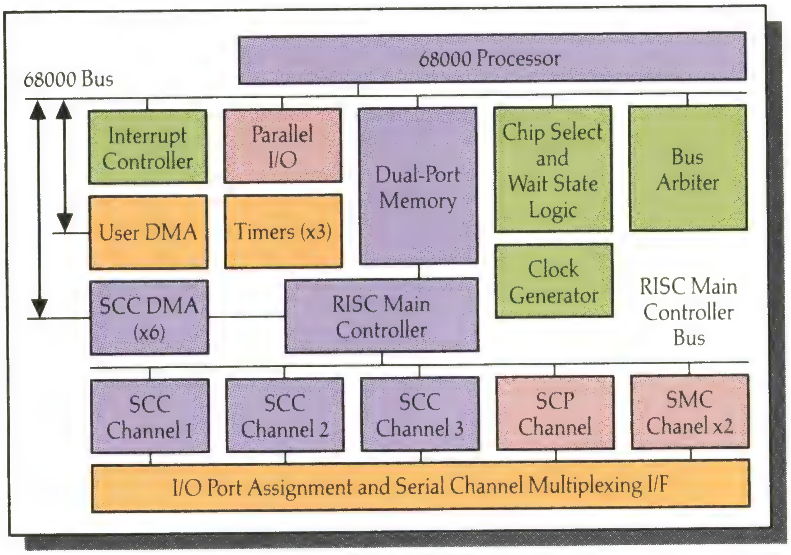
NOW A WORD ABOUT THE ECONOMY.

To save you even more money (and a bit of board space), the 68302 is the most highly integrated communications controller around. In addition to its mighty processors, it comes with a system integration module that's loaded with system glue logic (see diagram for details) you'd otherwise have to provide yourself.



COMMUNICATE TOLL FREE.

So whether you're designing for ISDN or any other form of communication, you simply can't do any better than the 68302.

For more information on the 68302, the third-party support behind it, and our 68302 Application Development Systems Evaluation Board, call 1-800-441-2447. Or contact the Motorola Semiconductor sales office nearest you.

It's sure to be the start of some great communication.

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	KM6165L	64K x 1	25/35/45ns	SDIP/SOJ
	KM6465	16K x 4	25/35/45ns	SDIP
	KM6465L	16K x 4	25/35/45ns	SDIP
	KM6865	8K x 8	35/45/55ns	SDIP
	KM6865L	8K x 8	35/45/55ns	SDIP
256K	KM61257	256K x 1	25/35/45ns	SDIP/SOJ
	KM61257L	256K x 1	25/35/45ns	SDIP/SOJ
	KM64257	64K x 4	25/35/45ns	SDIP/SOJ
	KM64257L	64K x 4	25/35/45ns	SDIP/SOJ
	KM68257P	32K x 8	35/45/55ns	DIP
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1Mb	Now in development			

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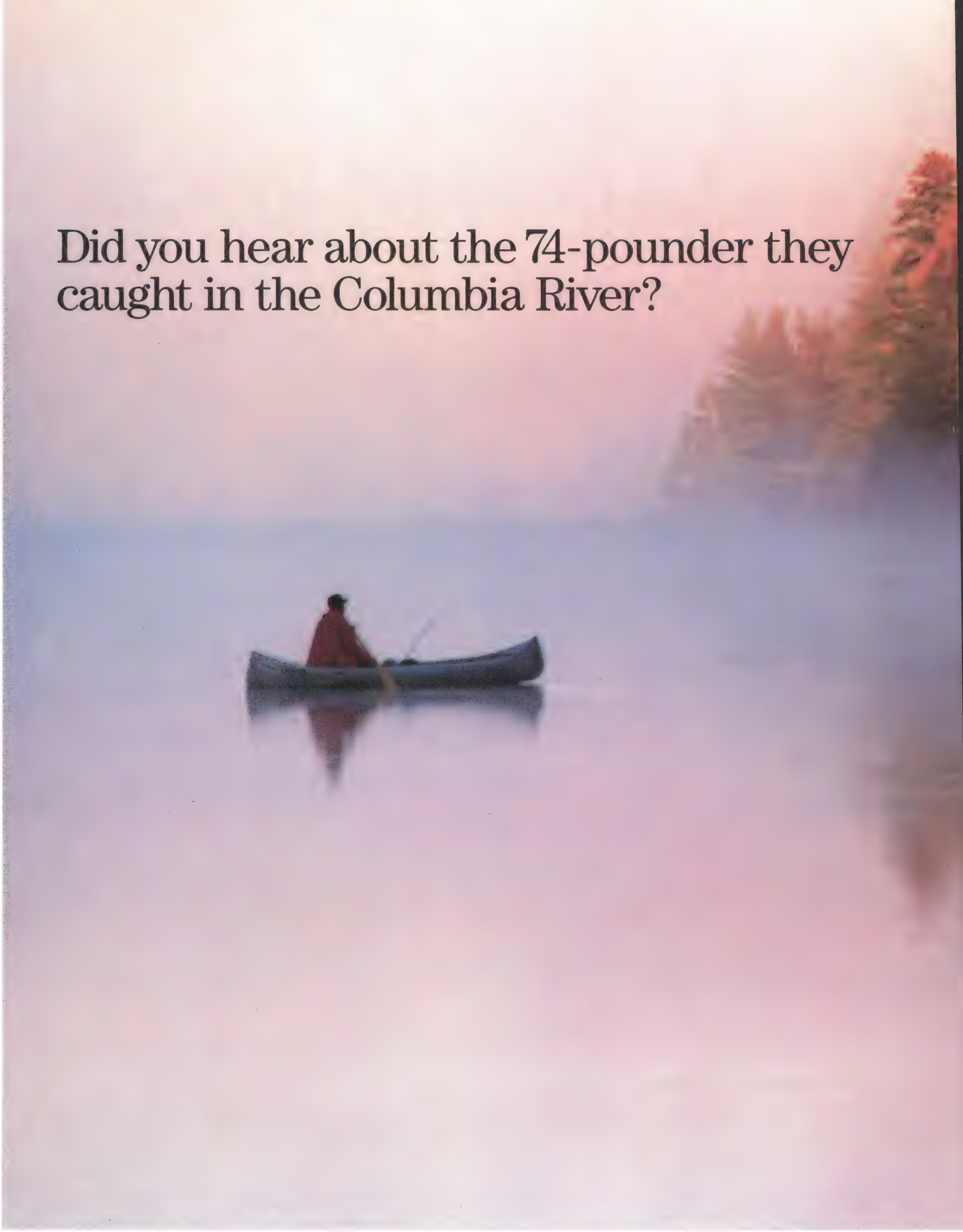
Did you hear about the 74-pounder they caught in the Columbia River?

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It worked without a snag.

This is a story about the one that got away. And then came back as reliably as ever.

In 1987, bandits stole four HP signal generators from a truck in Spokane, Washington. Luckily, police managed to recover three of them. But the last one disappeared without a trace.

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But rather than clean this catch, one of our Service Engineers decided to plug it in. To his surprise, the instrument emitted a signal. Even more remarkable, it met specifications.

Stories like this underscore why HP rates highest for reliability among engineering managers. We're still not satisfied. In fact, in 1979 we started a Total Quality Control program to increase quality ten-fold in 10 years. We'll reach that goal this year.

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CIRCLE NO. 35

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

STD BUS MODULE HOSTS IBM PC/AT CPU, MEMORY, AND I/O

The CPU-AT from Computer Dynamics Sales (Greer, SC, (803) 877-8700) replicates all the functions typical of an IBM PC/AT-compatible computer on a single STD Bus module. Two back-to-back pc boards make up the 1.4-in.-thick module. The primary board includes an 80C286 µP, BIOS, and as much as 4M bytes of RAM. The second board hosts floppy- and hard-disk controllers and your choice of flat-panel-compatible graphics controllers. The module runs the MS-DOS and Unix operating systems, but you can also embed it in applications without an operating system. A board with a 10-MHz µP, 512k bytes of RAM, CGA graphics, and a disk interface costs $1995 and will be available in May.—Maury Wright

SOFTWARE SCREENS PHYSICAL DESIGNS FOR CROSSTALK

BoardScan from Quantic Laboratories (Winnipeg, Canada, (800) 665-0235) screens pc-board designs for crosstalk and other transmission-line problems. The software runs fast enough to let you analyze a complete design. You can analyze the potential problem areas the software finds in detail with the Greenfield transmission-line-analysis products already available from the company. BoardScan will be available in the third quarter of 1990 for $14,000.—Doug Conner

IC IMPLEMENTS PROPOSED IMAGE-COMPRESSION STANDARD

An IC from C-Cube Microsystems (San Jose, CA, (408) 944-6300) can help designers win back much of the memory and data bandwidth commandeered when a computer handles photographic images. The CL550-27 can compress or decompress images as fast as 40M bytes/sec with a compression ratio of 8:1 to 200:1. These rates are fast and dense enough to let you store three minutes of compressed video on a 20M-byte hard-disk drive and record or play back the data at the video rate of 30 frames/sec. The CL550 implements the proposed JPEG (Joint Photographic Experts Group) image-compression standard, as defined by the CCITT/International Standards Organization.

The chip handles RGB (red, green, blue), YUV (luminance/chrominance), and CMYK (cyan, magenta, yellow, black) data with equal facility. You can connect it directly to a 16- or 32-bit host processor. Because the standard requires 8×8-pixel blocks of data, the chip also provides control signals for the 8-line external buffer you'll need for raster-scan video. The chip comes in a 144-pin pin-grid array or quad flatpack. Samples will be available in June, with full production scheduled for September. System designers can obtain an OEM developer kit containing an engineering sample, design notes, and software drivers for $550 now. Devices cost $155 (10,000). The company also offers a software implementation of the standard for $500.
—Richard A Quinnell

GATE ARRAY REPLACES MULTIPLE 7-NSEC PLDs

The GaAs PLR2KT gate array from Vitesse Semiconductor (Camarillo, CA, (805) 388-3700) offers high integration and high speed suitable for 33-, 40-, and future 50-MHz µP-based systems. With an internal flip-flop toggle rate of 1 GHz, any pin-to-pin function requires approximately 7 nsec. The TTL/CMOS-compatible I/O has a bandwidth of 150 MHz. The $45 (1000) array features 2400 2-input NOR gates and 92 signal I/O pins, roughly six times that available with the PAL16R8-7 7.5-nsec PLD. The array requires 1.5W typ and 2.8W max, which is less than half the power required by six PAL16R8-7s. The device's 132-pin quad flatpack has a built-in heat sink and requires 2 in.^{2} of board space. The company will automatically convert your PLD source files using Snopsys logic-synthesis design tools, or you can use traditional gate-array design methods.—Anne Watson Swager

CHIP SET FILLS DATA AND FAX MODEM NEEDS

The XR-2900 2-chip set from Exar Corp (San Jose, CA, (408) 434-6400) can perform V.22 bis 2400-bps full-duplex data communications and V.29 9600-bps half-duplex fax communications. The chip set includes the XR-2901 DSP μP and the XR-2902 combination digital and analog front-end chip. The chip set implements analog and remote- and local-digital test facilities. Other features include a DTMF generator, an automatic adaptive equalizer, a guard-tone generator, and a call-progress monitor mode. The chip set costs $27.33 (10,000).—Maury Wright

DSP SYSTEM ACCELERATES TO 33M FLOPS

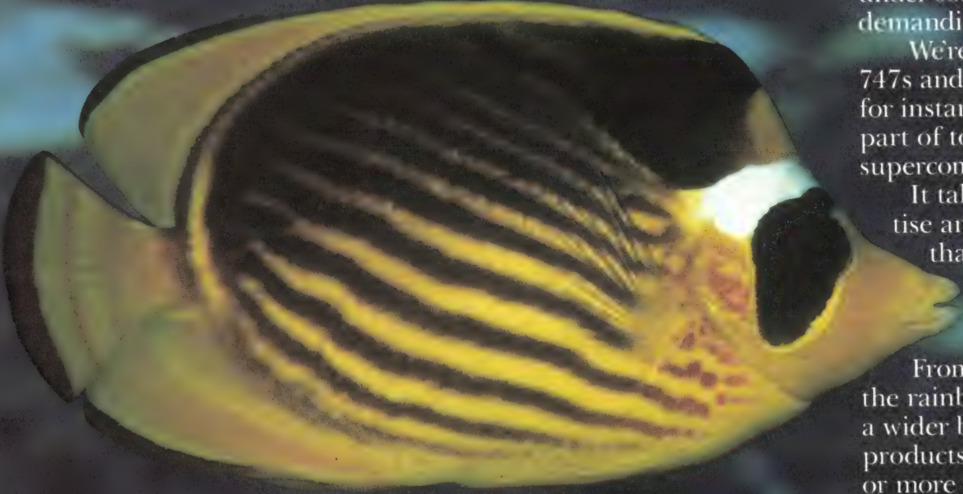
The TMS320C30-based DSP board from Loughborough Sound Images (Loughborough, UK, (0509) 232843) includes memory and I/O expansion and has software support. The TMS320C30's clock speed is 33 MHz, which, under ideal conditions, can perform 33M flops. The board plugs into an IBM PC/AT or compatible computer. The board adds 1M byte of static RAM (SRAM), twin 8.3M-bps serial links, and two 16-bit A/D channels. The A/D channels' sample rate is 200k samples/sec. The standard 32-bit-wide memory consists of 128k words of 25-nsec, zero-wait-state SRAM. Of this memory, 64k words are dual-ported memory. A memory-expansion port connects to additional 4M-word memory boards. A 16-bit, 5M-sample/sec, bidirectional parallel interface accesses adjacent plug-in boards or your custom I/O. As well as an assembler, a linker, and a C compiler, the software support pack provides a C-interface library. The PCS/320C30SP DSP board and software costs £3995; the PCM/320C30 4M-byte memory board costs £1495.—Brian Kerridge

VOICE-ACTIVATED TYPEWRITER HAS 30,000-WORD VOCABULARY

The DragonDictate voice-activated typewriter recognizes 25,000 commonly used words and an additional 5000 user-defined words, which can include proper names, company names, and technical terms. The system consists of an 8-bit ISA bus card, a noise-canceling headset microphone, and voice-recognition software. The software can recognize speaker-independent words or utterances of less than 5-sec duration that are separated by 0.25-sec pauses. The system then prints each recognized word or utterance on the display.

If the system is unsure of a word, it displays a window highlighting the most likely candidate along with a listing of other possible candidates. If the most likely candidate is the correct word, the user continues dictating. If the correct word is in the list, the user selects the word by dictating the appropriate word number, such as "Choose 2." If the word isn't on the list, the user can spell the word using the International Communication Alphabet—alpha for "a" and charlie for "c." The

Thanks to us the government knows this is not an enemy sub.



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system puts the word in the user-defined area for future use. Each user generates a voice-recognition model based on his or her speech pattern; the system calls this model when the user logs on. The $9000 system requires an 80386-based computer, a 1.2M-byte, 5¼-in. floppy-disk drive, 640k bytes of standard memory, 7M bytes of extended memory, and a hard-disk drive with 8M bytes of free space.
—John A Gallant

LOWER POWER, WIDER VOLTAGE RANGE FOR ECL

National Semiconductor Corp's (Santa Clara, CA, (408) 721-5000) F100K 300 Series is a lower-power version of 100K ECL. The devices operate from −4.2 to −5.7V and use 30 to 50% less power than the 100K devices they replace. Due to their extended voltage range, you can use 300 Series devices with 10K, 100K, and 10KH ECL. You can also run the devices with reverse polarity power and connect them directly to TTL. The first devices in the series include byte-wide gates, inverters, translators, buffers, and latches. They are available in ceramic DIPs, flatpacks, and plastic chip carriers, and prices start at $4.85 (100).—Richard A Quinnell

SAMPLING CONVERTERS PROLIFERATE

Manufacturers of hybrid sampling converters—devices that package a S/H amplifier with an A/D converter—continue to offer new options. Micro Networks (Worcester, MA, (508) 852-5400) has introduced a 12-bit, 2-MHz converter. The MN6249 combines the company's MN5249 400-nsec A/D converter with the MN376 200-nsec track-and-hold amplifier. The 40-pin triple-wide DIP consumes 3.5W typ and is available in different performance and specified-temperature ranges. Prices range from $285 to $571.50 (100).

Datel (Mansfield, MA, (508) 339-3000) has introduced a midrange sampling-rate converter. The ADS-131 adds a 12-bit, 5-MHz option to more standard 12-bit converters that sample at 2 or 10 MHz. The company characterizes the ADS-131 as high as the Nyquist rate of 2.5 MHz. Dynamic specifications include a total harmonic distortion of −70 dB, a S/N ratio with distortion of −66 dB, and an input bandwidth of 65 MHz. Also available in a 40-pin triple-wide DIP, this sampling converter consumes 3.65W typ. The commercial-temperature-range model costs $439; the military model costs $508 (100).—Anne Watson Swager

REAL-TIME OS KERNEL SUPPORTS 80860 µP

JMI Software Consultants Inc (Spring House, PA, (215) 628-0846) has announced a version of its real-time C Executive operating-system kernel for Intel Corp's 80860 µP. The C Executive is a real-time, multitasking kernel and supplies standard I/O lines, a re-entrant C library, and device drivers, all of which are written in C. An unlimited-use licensing fee for a single processor type costs $25,000; you can add additional processor licenses for $5000 each.—Steven H Leibson

COMPANY LOWERS PRICES OF FLASH A/D CONVERTERS

As a result of reduced manufacturing and handling costs, Datel (Mansfield, MA, (508) 339-3000) has lowered the price of its family of 8- and 10-bit flash converters by 24 to 74%. Most drastically reduced are the prices of the 8-bit 50M-sample/sec ADC-302 and 100M-sample/sec ADC-303 converters. The company reduced their prices from $215 and $550 to $55 and $148, respectively.—Anne Watson Swager

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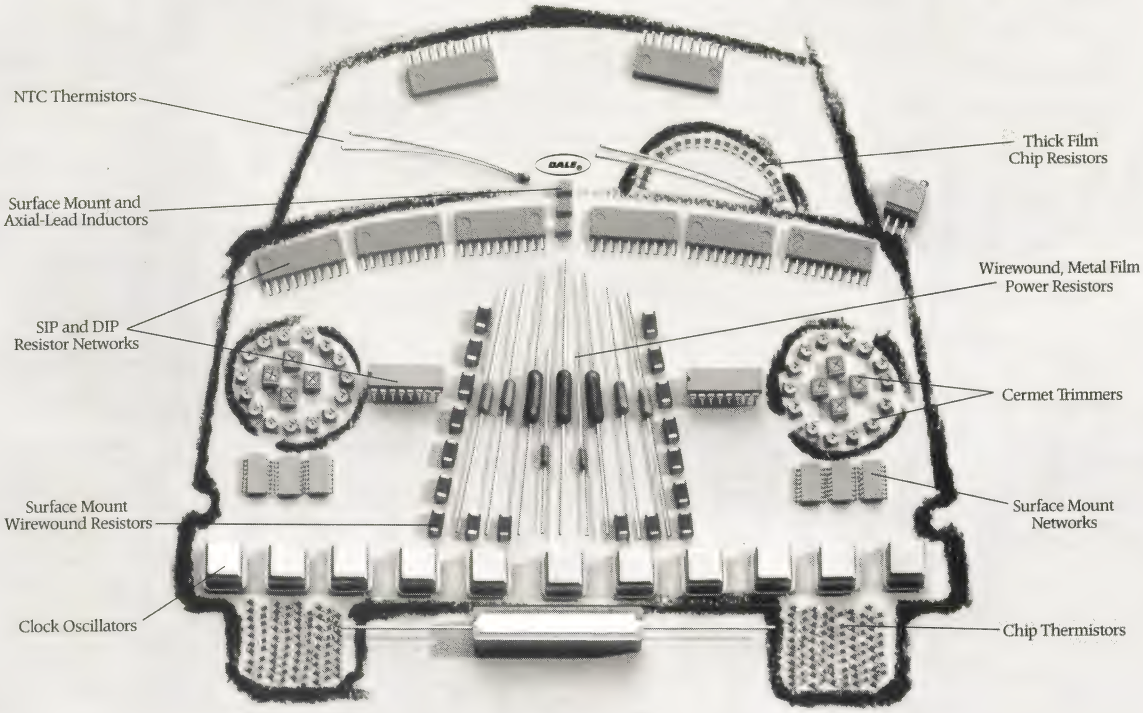
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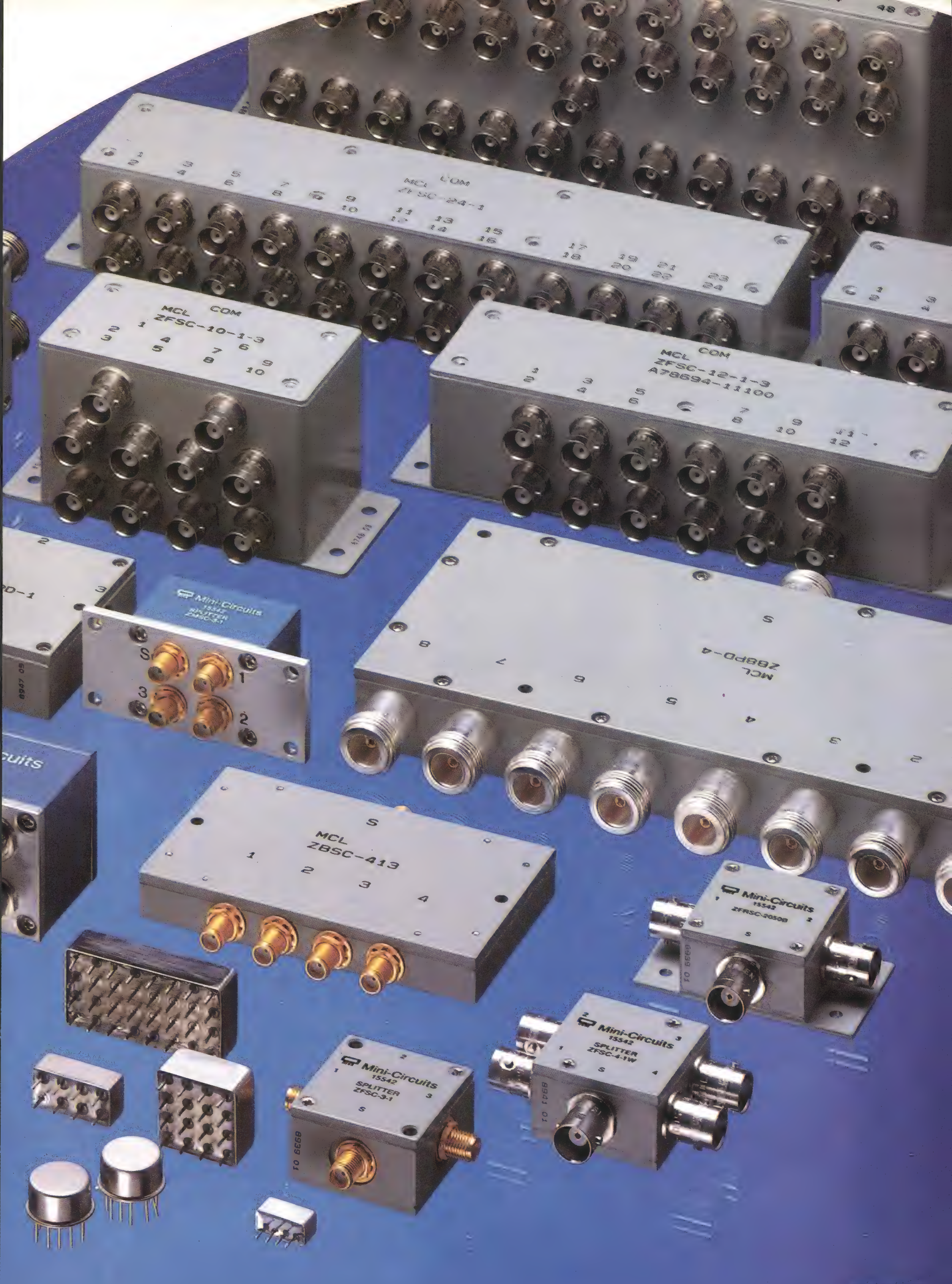

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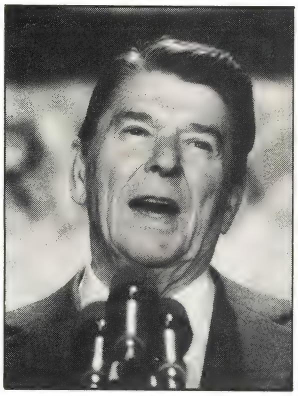
In 1979, Margaret Thatcher is voted in as Prime Minister of Great Britain…

and EDN is voted #1 in readership.

In 1980, Ronald Reagan is elected President of the United States…



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In 1982, Yuri Andropov is elected as the leader of the USSR…

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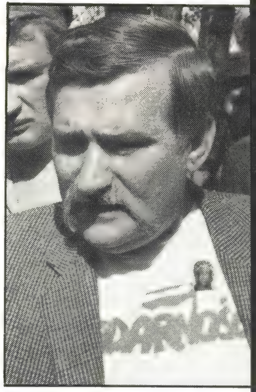
In 1983 Lech Walesa of Poland wins the Nobel Peace Prize…



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Apex Technology	**#1**	5
Sipex Corporation	**#1**	4
Kyocera Northwest, Inc.	**#1**	NOT INCL.

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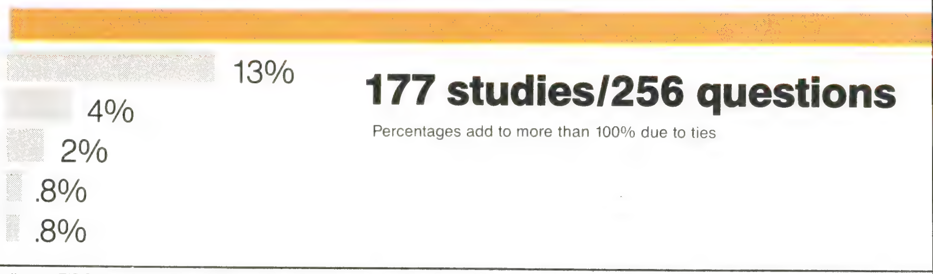

EDN	
Electronic Design	13%
Electronic Products	4%
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Electronics	.8%
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177 studies/256 questions

Percentages add to more than 100% due to ties

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*Independent studies are conducted across customer/prospects lists or TIDS lists, not across a magazine's or newspaper's own list, which results in obvious bias. **Results based on the question

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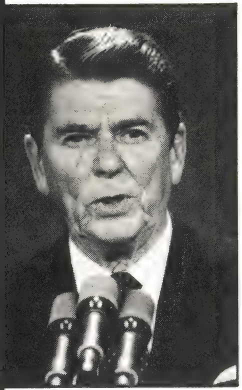

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In 1986, Corazon Aquino
is chosen as the President
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In 1987, Margaret Thatcher
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2	4	3	NOT INCL.
4	3	2	NOT INCL.
2	4	3	6
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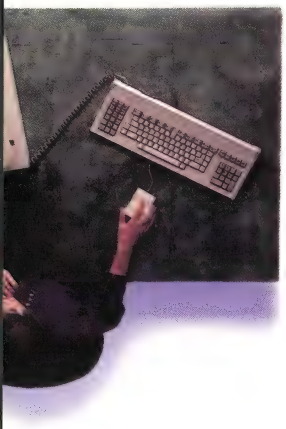

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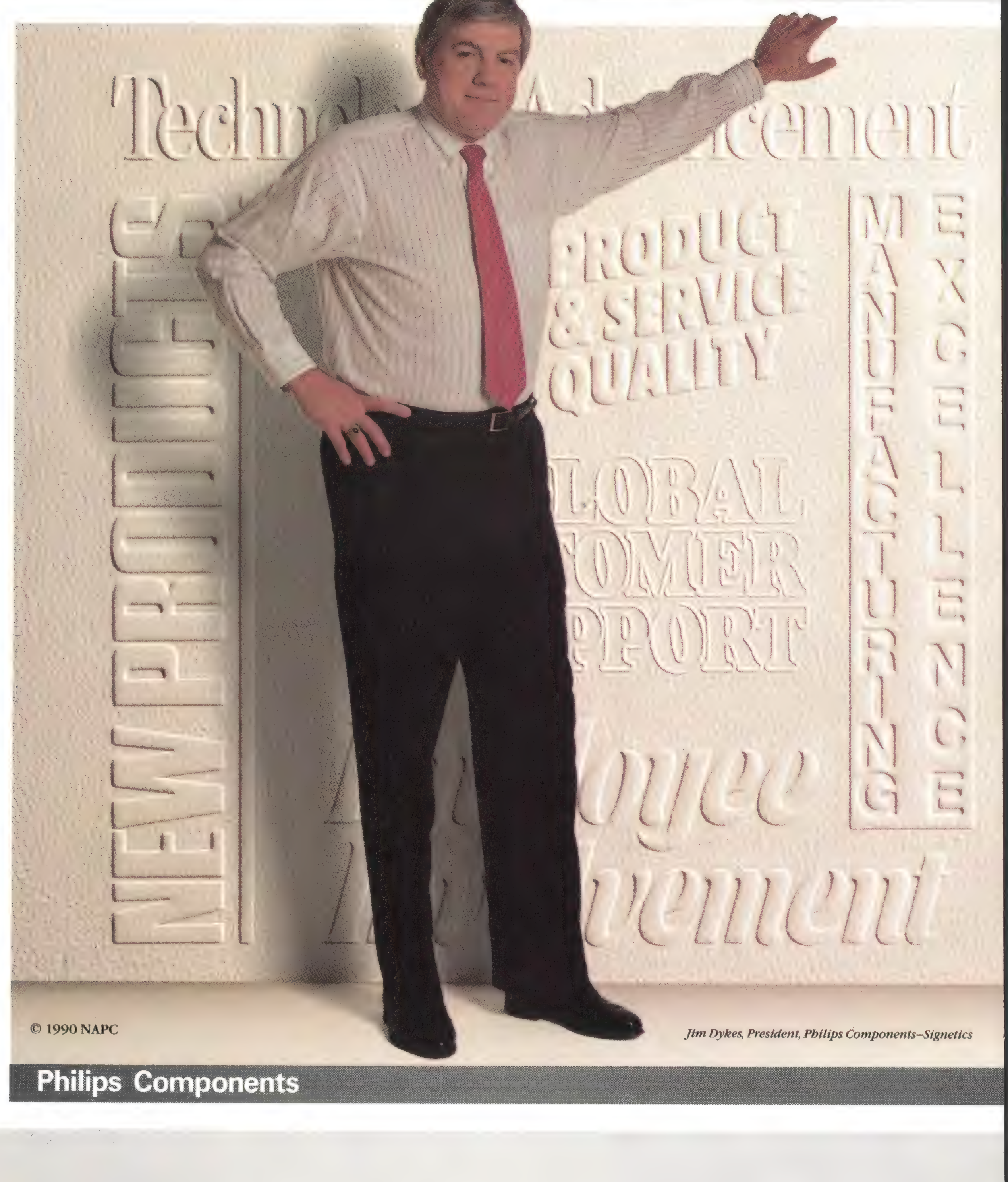

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Jim Dykes, President, Philips Components–Signetics

Philips Components

# of performance by which will be measured.”

JIM DYKES ON MAKING THE PREFERRED LIST.

As IC markets advance into the ’90s, benchmarks are shifting from speed and specs to new global criteria. Customers are narrowing their suppliers to a few key partners who excel in six essential areas. Here’s how Signetics is responding to these six “dimensions of performance.”

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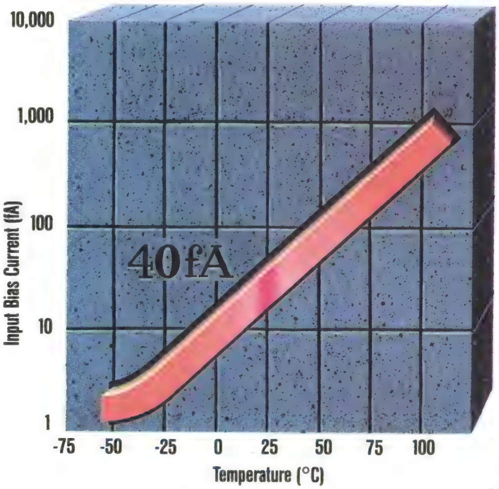

INPUT BIAS CURRENT VS. TEMPERATURE: 40 fA AT 25°C

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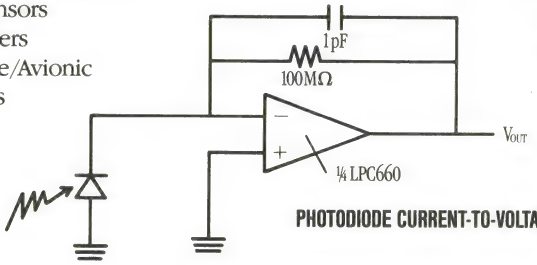
In the past, a single-supply op amp was an amplifier whose input common-mode range included ground. But in today's +5V systems, you need op amps that take advantage of every last volt that the supply provides, and whose outputs swing fully from rail-to-rail. National was the first to deliver rail-to-rail performance with the LMC660 and now has a complete family—all in CMOS.



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Help needed to rebuild library

Please let me introduce myself: I am a senior engineer at the Institute for Atomic Physics in Bucharest, Romania, and co-author of several books on optoelectronics and optical information. I am writing this letter to call your attention to a tragic event that occurred in Bucharest during the democratic revolution of December 22, 1989: the University Central Library was completely destroyed by fire.

I am asking for the support of your readers and other interested parties in helping to rebuild the library, according to their abilities. The library needs donations of books, conference proceedings, student text books, journal collections, lecture notes, and other materials in the fields of mathematics, physics, chemistry, engineering, medicine, and human and natural sciences. Their help will be gratefully acknowledged.

Dan G Sporea
Box 31-53
Bucharest, Romania

Address corrections

Due, in part, to errors in Apple Computer's Engineering/Scientific Solutions Winter 1989/1990 Guide, many of the addresses and phone numbers provided in the Special Report on Macintosh-based CAE (EDN, March 1, 1990, pg 138) were inaccurate. Below are the corrected addresses and phone numbers.

Algorithmic Systems, 399 Pond St, Number C5, Braintree, MA 02184. (617) 849-0580. **Circle No. 734**

Bobcat Systems Inc, Box 2596, West Chester, PA 19380. (215) 696-6286. **Circle No. 735**

BrainPower Inc, 30497 Canwood St, Agoura Hills, CA 91301. (818) 707-1712. **Circle No. 736**

Deutsch Research, 761 DeSoto Dr, Palo Alto, CA 94303. (415) 327-8677. **Circle No. 737**

Doctor Design, 5415 Oberlin Dr, San Diego, CA 92121. (619) 457-4545. **Circle No. 738**

Imagine That Inc, 7109 Via Carmela, San Jose, CA 95139. (408) 365-0305. FAX (408) 629-1251. **Circle No. 739**

Intusoft, Box 6607, San Pedro, CA 90734. (213) 833-0710. FAX (213) 833-9658. **Circle No. 740**

MicroSim, 20 Fairbanks, Irvine, CA 92718. (714) 770-3022. **Circle No. 741**

San Juan Software Co, Box 27620, Seattle, WA 98125. (206) 367-4188. **Circle No. 742**

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Vamp, 6753 Selma Ave, Hollywood, CA 90028. (213) 466-5533. **Circle No. 745**

Reader refers to voltage references

In the Special Report on voltage references (EDN, January 18, 1990, pg 120), I thought the subject was covered very well. I have only one thing worth adding that might be helpful to a circuit designer using voltage references.

Because references are noisy, quite often one wants to put a cap directly across the output dc level. This operation usually works except when the part is an active device with low output impedance. Oscillations can result with disastrous effects. An example is the emitter-follower oscillator. These oscillations can be up in the FM band. Even a careful designer can miss it on the bench when looking for dc circuit problems. One manufacturer, National Semiconductor in fact, states its LM113 specification in Note 2: "...should not be operated with shunt capacities between 200 to 0.1 pF...as it may oscillate at some currents."

It would pay to check with the manufacturer before putting decouplers directly on outputs of references. Decoupling input raw dc voltage close to the device is usually a good practice, because references are often active devices. We had a lovely 10-MHz oscillation on production boards where the decoupler was at the other end of a 10-in. pc-board trace from an 18V IC reference.

David M Weigand, PE
West Chester, PA

Industrial PC omissions

EDN regrets the omission of the following vendors from the article, "Harsh conditions affect industrial PC design" (EDN, January 4, 1990, pg 45): Amdex Corp, 17B Corporate Place, 267 Boston Rd, North Billerica, MA 01862, Phone (508) 663-2070, FAX (508) 663-5094; and Video Graphic Systems, 4163 St Clair Ave, Studio City, CA 91604, Phone (818) 509-5738, FAX (818) 509-8866.

Both of these companies manufacture industrial PCs that qualify for inclusion in the article's table.

Reader questions "empirical" approach

I normally enjoy reading Jim Williams' articles because he has a real creative ability to develop innovative applications for his company's products. The latest one, however, "Basic principles and ingenious circuits yield stout switchers" (EDN, January 18, 1990, pg 151), really caused me some concern. Jim states at the beginning of this article that switching regulators may be designed by following some basic principles, and then he says, "Because of the overwhelming level of difficulty associated with magnetic components ...an empirical approach is often the best way to select inductors."

Granting that most designers, myself included, may not be as familiar with Ampere's and Faraday's laws as we are with Ohm's law, magnetics is not that much of a black art. When I read Jim's suggestion that you may select an appropriate inductor by feeling its weight and measuring its dc resistance, I don't know whether to laugh or cry. If Jim is putting us on, he is a very funny writer, but it's a sad day for engineering if readers get the impression that this is an acceptable method for designing reliable switching regulators.

Specifying an inductor is not a trivial task but neither is it "overwhelmingly difficult." The equations are simple and readily available in probably hundreds of sources ranging from textbooks to manufacturer's application guides. I'm sorry to criticize, but to ignore all this in an article about "basic principles" does a disservice to our profession.

Robert A Mammano
Vice President
Advanced Technology
Unitrode IC Corp
Santa Ana, CA

(The author's reply: I appreciate Robert Mammano's taking the time to write. I hope my reply will clear up any confusion.

I think it's important to examine the complete content and precise wording of the article, so I refer you to reading the text surrounding the suggestions Robert refers to. (See the entire section under the subhead, "The invasion of the drawer dwellers," pg 152.) The particular sentences that sharpen the focus of the context read: "An alternate inductor-selection method exists—one favored by those who have no inductor kit, time, or adequate instruments. You can use this alternate method when faced with an immediate deadline and a drawer full of inductors of unknown or questionable lineage." "Although this method's theoretical underpinning is perhaps questionable, its seemingly limitless popularity compels coverage." "Inductors passing both stages of the test have an excellent chance (75%—based on a sample of randomly selected inductors) of performing adequately in

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a prototype circuit."

I think my suggestions in their original and complete form restore balance to their presentation. In particular, the majority of switching-regulator users have little experience in the area. More significantly, many do not desire to develop a substantial expertise. This observation doesn't make them poor or irresponsible engineers, but simply reflects their priorities. What they do want are concepts directly applicable to construction of working circuits with readily available parts.

The area of switching regulators is the most difficult application area I have worked in. To a large extent, the difficulty lies in the subject matter. Switchers are hard. Because of this, high levels of user trepidation are common. If the goal is to get designers to utilize switching technology, one way to begin is to make them feel comfortable about it. The section Robert questions was written with tongue-in-cheek, but not too firmly planted there! Fully 90% of switcher-customer inquiries I handle involve magnetic-selection difficulties. These engineers are often anxious to prototype a feasible solution to their problems. I want to ensure that their initial efforts are encouraging, not disheartening. It's much easier to work with and get enthusiastic about a functional circuit than one that doesn't work.

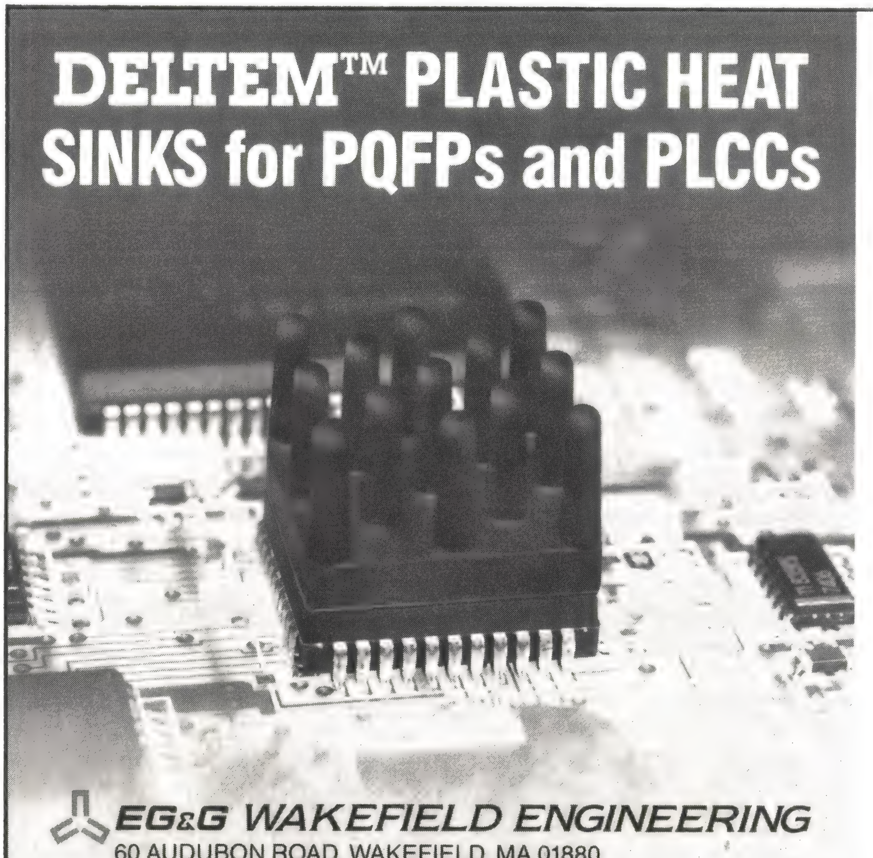
When writing technical material, I try to appeal to a broad section of the engineering population. The interest level and expertise spectrum of the audience varies considerably. A cardinal error is to assume that the most interested people possess a high degree of familiarity with the subject matter. This assumption is simply not true. As such, it is my responsibility as a writer to try to communicate with both aficionados and newcomers. I can't say I'm always successful at doing this, but it's the goal.

I'm sorry Robert Mammano didn't find this balance in my presentation, and I welcome his suggestion on how to achieve it.)

Company name omitted

The following company name and address was inadvertently omitted in the article on thermal-analysis software (EDN, February 1, 1990, pg 47): W F Chew Enterprises, 717 W 14th St, Long Beach, CA 90813. (213) 432-2704.

EDN



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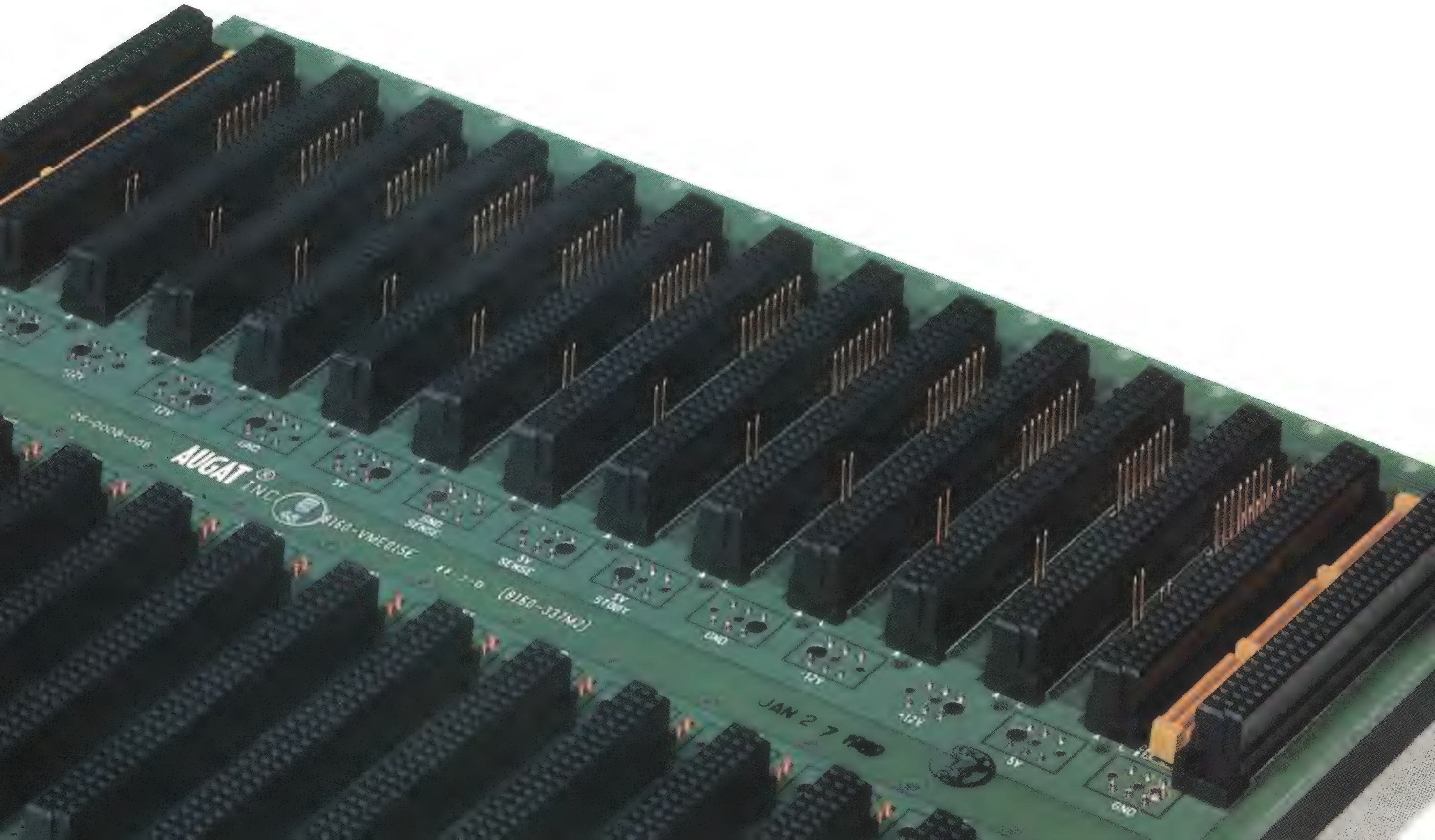

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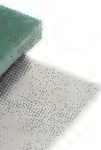

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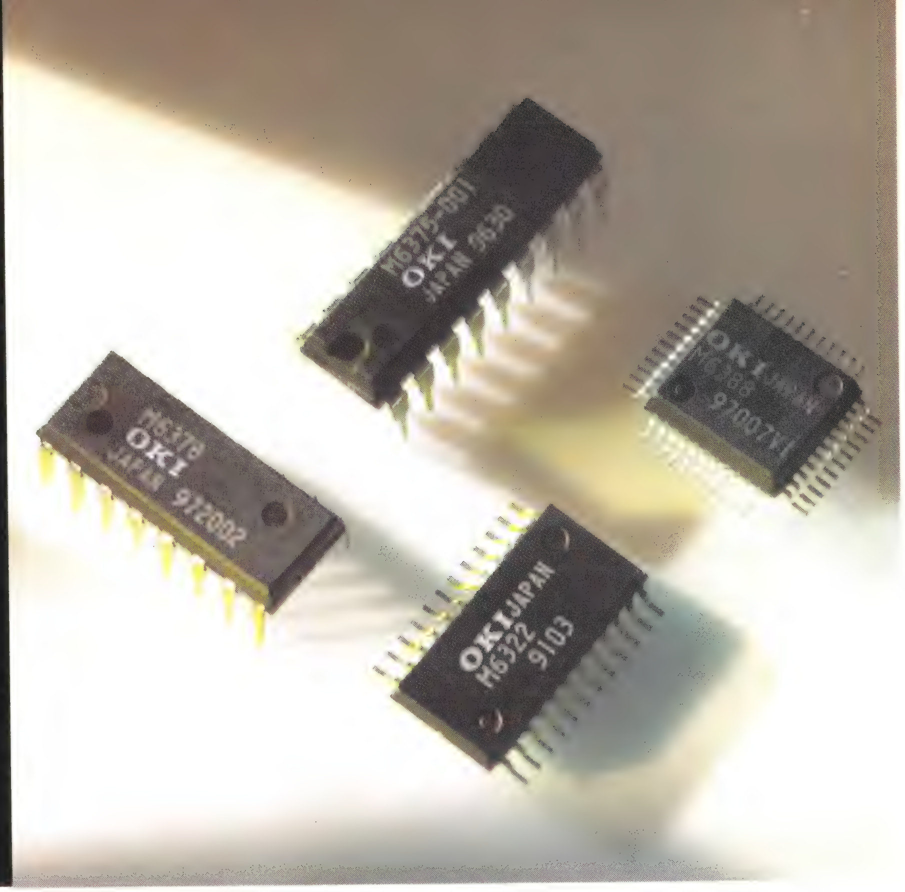

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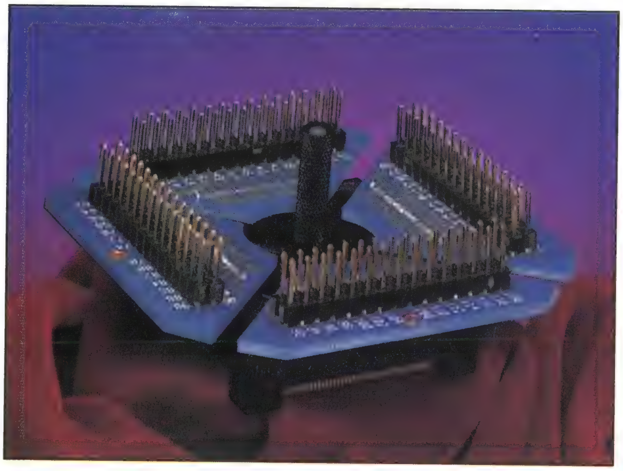

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CALENDAR

1990 Technical Symposium on Optical Engineering and Photonics in Aerospace Sensing/Exhibit, Orlando, FL. SPIE, The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX (206) 647-1445. April 16 to 20.

Laser Technology Application in Manufacturing Update—1990, Sunnyvale, CA. Roger W Hirons, Center for Continuing Engineering Education, 929 N Sixth St, Milwaukee, WI 53203. (414) 227-3100. April 17 to 18.

VME Computer Expo/Seminar, Minneapolis, MN. James R Johnson and Associates, Computer Products Div, Box 41004, Plymouth, MN 55441. (612) 478-9442. FAX (612) 478-6186. April 17 to 18.

DOD-STD 2167A/2168, San Diego, CA. David Maibor Associates Inc, Box 846, Needham Heights, MA 02194. (617) 449-6554. April 17 to 19.

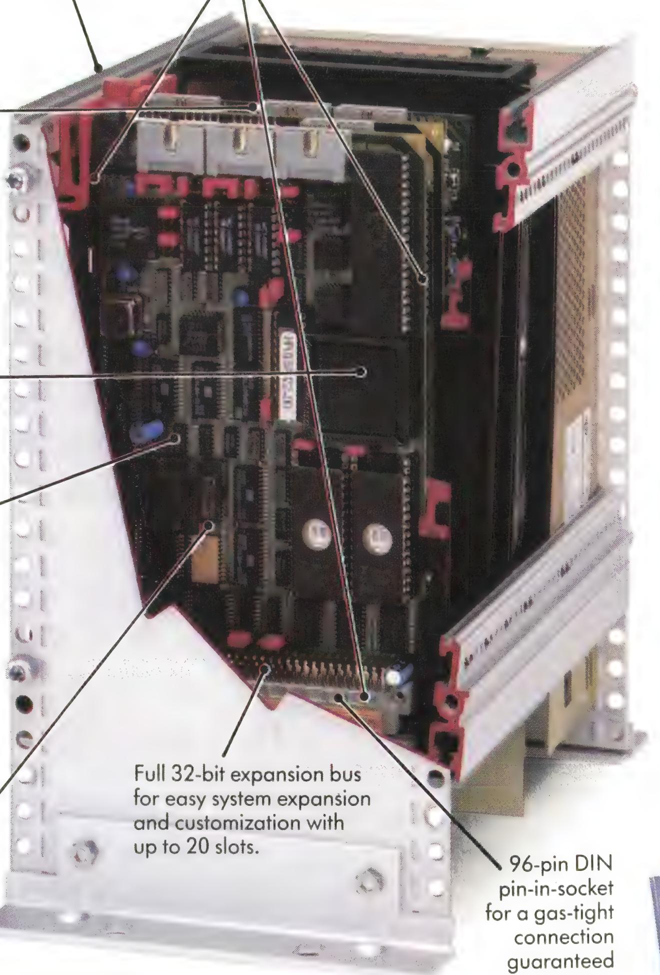
Grounding and Shielding (short course), Washington, DC. Interference Control Technologies, Box D, Gainesville, VA 22065. (703) 347-0030. April 17 to 20.

SECSII for SMT Automation (short course), Bethlehem, PA. National Training Center for Microelectronics, Northampton Community College, 3835 Green Pond Rd, Bethlehem, PA 18015. (215) 861-5450. FAX (215) 861-5060. April 19.

Designing for Electromagnetic Compatibility (short course), Novi, MI. Hewlett-Packard Co, Signal Analysis Div, 1212 Valley House Dr, Rohnert Park, CA 94928. (313) 349-9200, ext 2448. April 19 to 20.

Electronics Packaging Technology (short course), East Brunswick, NJ. The Center for Professional Advancement, Box 964, East

At Last, a *Truly* Industrial PC AT System for the OEM



Easy to mount Eurocard hardware with optional power supply. Can be rack mounted or bolted into any embedded system.

Three side mechanical bond into the card cage, yet easy to access for simplified maintenance.

100% compatible EGA color display and AT keyboard interface.

Genuine Intel 80286, 10 MHz CPU, for true AT performance.

512K of fast access RAM, Clock/calendar, dual communication port and optional 80287 Arithmetic Unit on a very high density, two layer PC board.

Full 32-bit expansion bus for easy system expansion and customization with up to 20 slots.

Compact single height Eurocard board format (100 x 160 mm) that doesn't flex or bend and withstands the toughest shock and vibrations.

96-pin DIN pin-in-socket for a gas-tight connection guaranteed to last forever.

Unprecedented selection of inexpensive I/O functions, from the simplest parallel and serial I/O, to high performance networking, X.25, motor control and imaging.

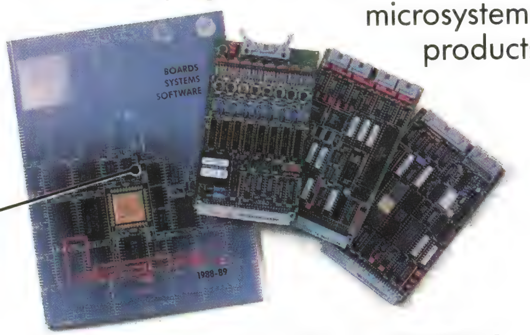
Introducing the first PC AT system originally designed to be embedded into your machinery or instrumentation.

With the GESPAC AT system, ''ruggedized PC'' no longer describes a desk top PC in a stronger black box. Rather it is an architecture made to last by design, with such features as small and robust board format, and ultra-reliable pin-in-socket DIN connector.

What's more, the GESPAC System is built for performance with Intel's original 80286 processor and 80287 Arithmetic Unit — In fact this system is the most compact implementation of the 286 in the market today.

The powerful G-64 bus interface lets you customize your AT system with any of the 200-plus system components available from GESPAC, to match virtually any system requirement.

Take advantage of GESPAC's 10 years of experience in serving the OEM marketplace. Call today to receive your free data sheet and our new 116 page catalog of board level microsystem products.



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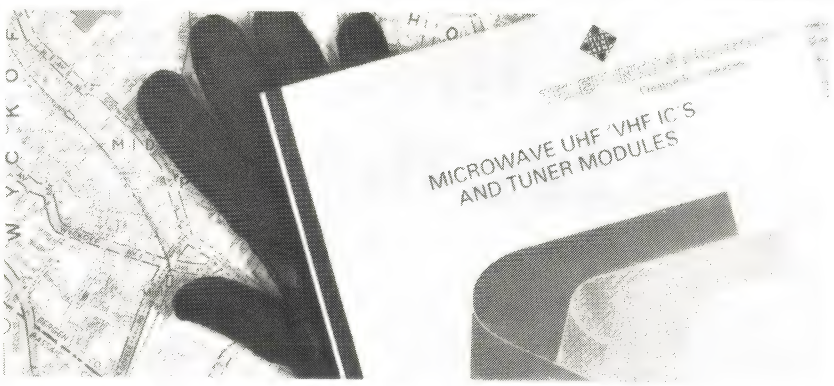
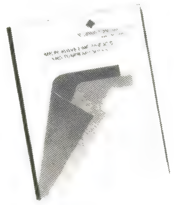
CIRCLE NO. 48



A Road Map to VHF, UHF & Microwave Component Design

Our "Atlas" is loaded with specs and engineering data describing Microwave UHF/VHF ICs and Tuner Modules. For information concerning Microwave Frequency Dividers (prescalers), PLL ICs, UHF/VHF front end ICs for communications, Video and FM Tuners, contact: AEG Corporation, 3140 Rte. 22, PO Box 3800, Somerville, NJ 08876-1269; (201) 231-8493; Fax: (201) 231-8353.



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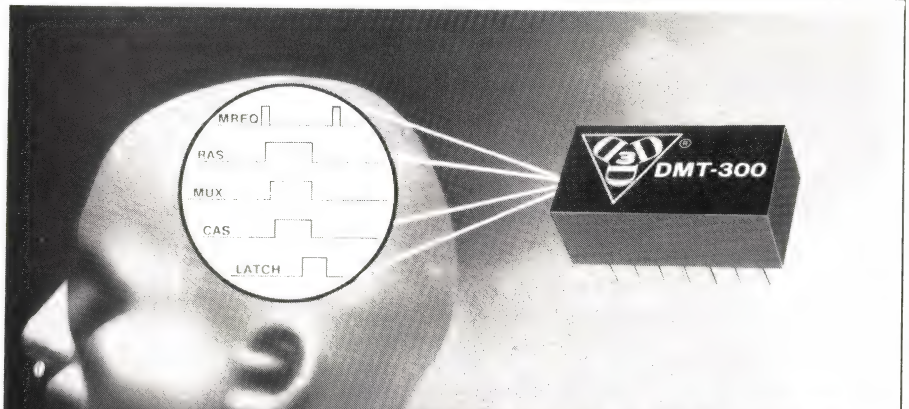

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Brunswick, NJ 08816. (201) 613-4500. FAX (201) 238-9113. April 23 to 25.

Solutions for High SMT Yields (short course), Bethlehem, PA. National Training Center for Microelectronics, Northampton Community College, 3835 Green Pond Rd, Bethlehem, PA 18015. (215) 861-5450. FAX (215) 861-5060. April 23 to 25.

1992 and the EEC Directive on EMC (short course), Chicago, IL. Interference Control Technologies, Box D, Gainesville, VA 22065. (703) 347-0030. April 24 to 26.

Designing for Electromagnetic Compatibility (short course), Naperville, IL. Hewlett-Packard Co, Signal Analysis Div, 1212 Valley House Dr, Rohnert Park, CA 94928. (312) 357-8800, ext 2253. April 26 to 27.

EMC Design and EMI Mitigation (short course), East Brunswick, NJ. The Center for Professional Advancement, Box 964, East Brunswick, NJ 08816. (201) 613-4500. FAX (201) 238-9113. April 30 to May 2.

Integrated Circuit Manufacturing Technology (short course), San Francisco, CA. The Center for Professional Advancement, Box 964, East Brunswick, NJ 08816. (201) 613-4500. FAX (201) 238-9113. April 30 to May 2.

Commercially Available Single-Chip Digital Signal Processors, Cambridge, MA. DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. FAX (617) 969-6689. April 30 to May 3.

Structured Development Forum XI, San Diego, CA. Computer Sciences Corp, 1321 Mercedes Dr, Hanover, MD 21076. (301) 859-0400. April 30 to May 3.

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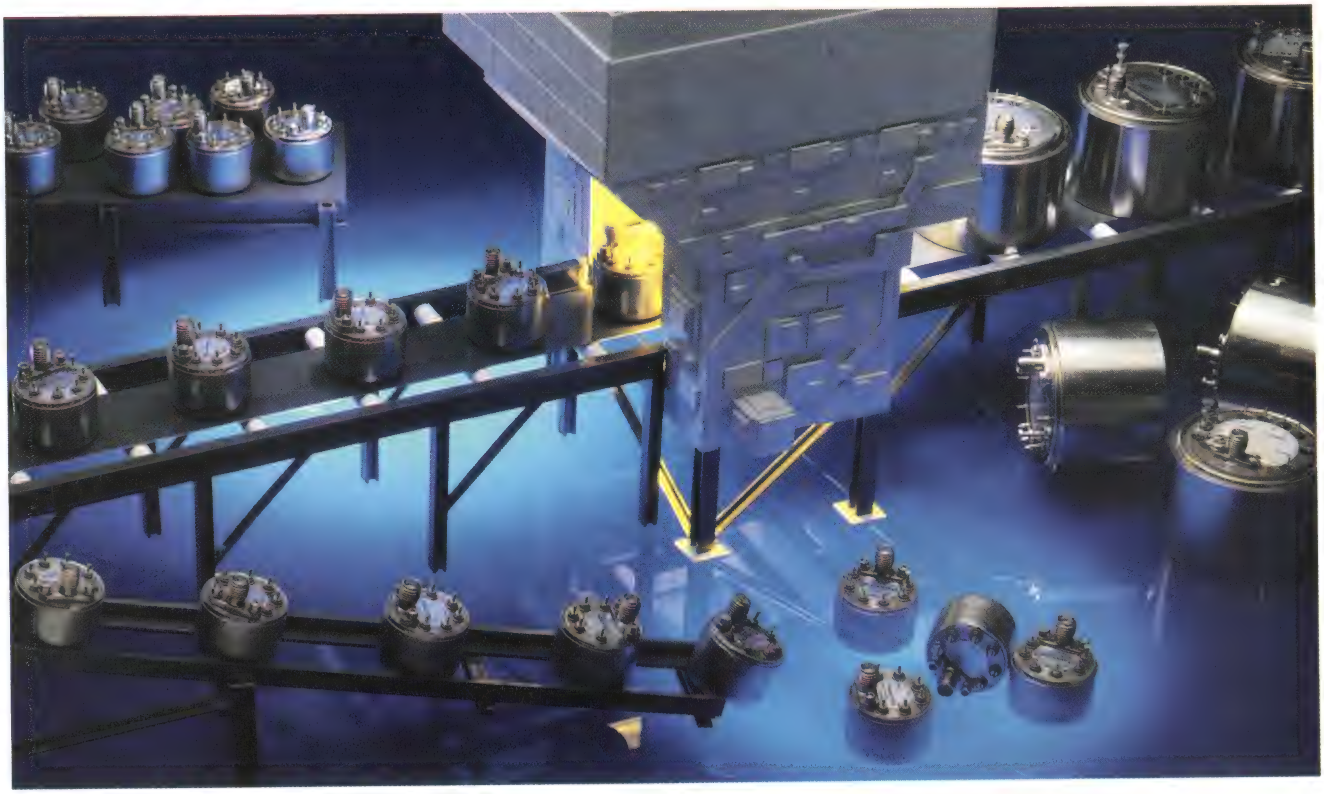

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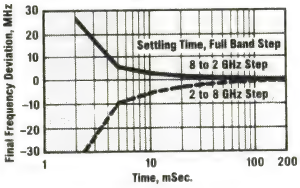

AV-7036 covers the 3.0 to 6.0 GHz range. AV-7028 provides 2.0 to 8.0 GHz frequency coverage. For both models, phase noise is typically −100 dBc/Hz at 20 kHz offset from carrier. And, power output is +13 dBm.

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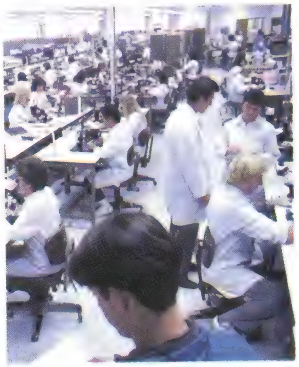

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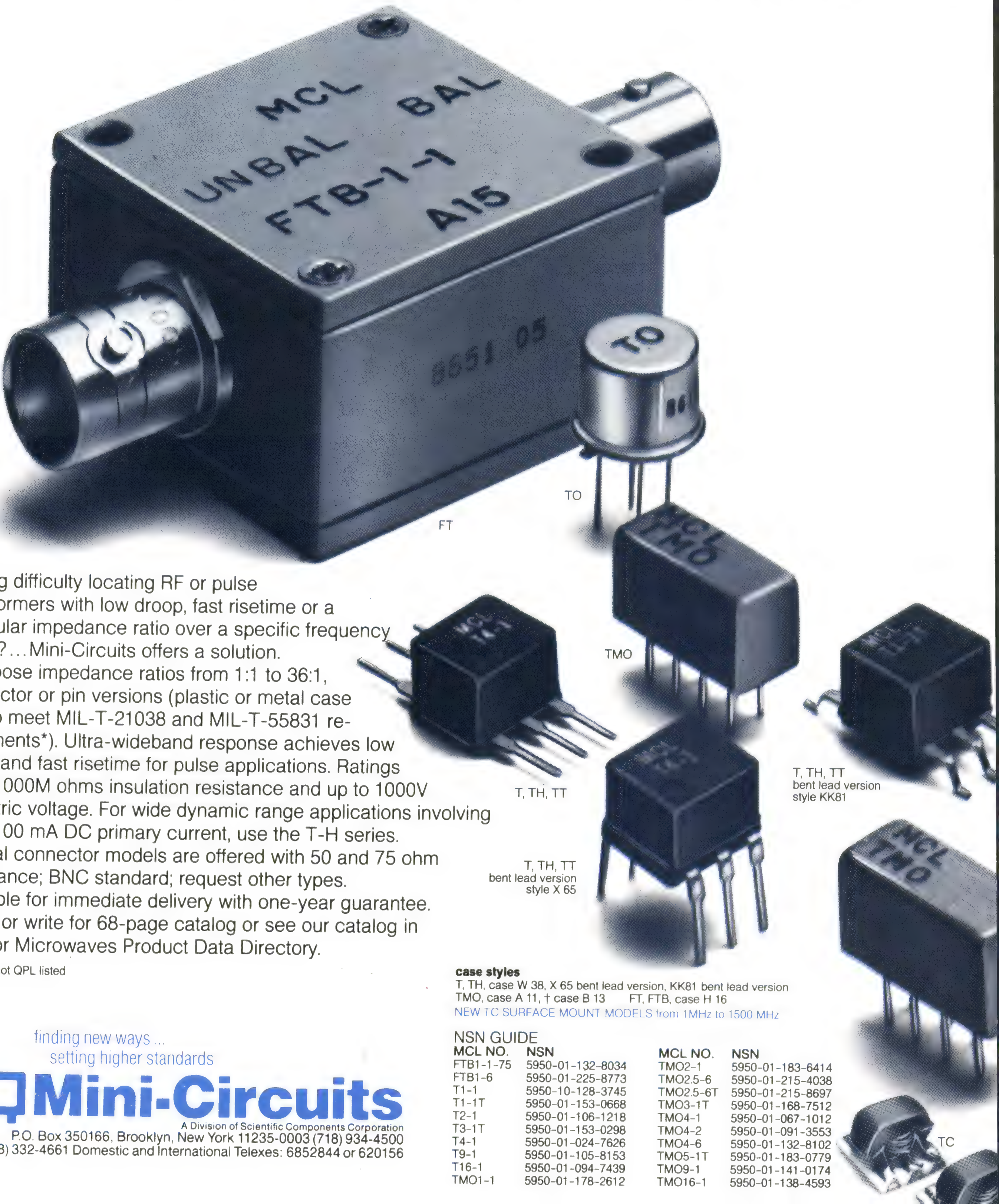
RF TRANS

Over 50 off-the-shelf models...



Having difficulty locating RF or pulse transformers with low droop, fast risetime or a particular impedance ratio over a specific frequency range?…Mini-Circuits offers a solution.

Choose impedance ratios from 1:1 to 36:1, connector or pin versions (plastic or metal case built to meet MIL-T-21038 and MIL-T-55831 requirements*). Ultra-wideband response achieves low droop and fast risetime for pulse applications. Ratings up to 1000M ohms insulation resistance and up to 1000V dielectric voltage. For wide dynamic range applications involving up to 100 mA DC primary current, use the T-H series. Coaxial connector models are offered with 50 and 75 ohm impedance; BNC standard; request other types. Available for immediate delivery with one-year guarantee.

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*units are not QPL listed

case styles
T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
TMO, case A 11, † case B 13 FT, FTB, case H 16
NEW TC SURFACE MOUNT MODELS from 1MHz to 1500 MHz

NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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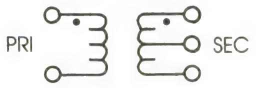
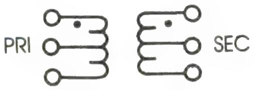
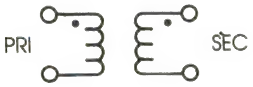
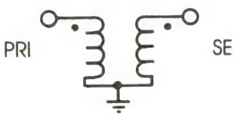
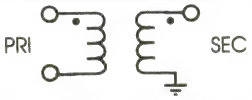
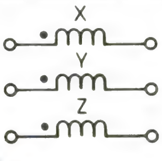
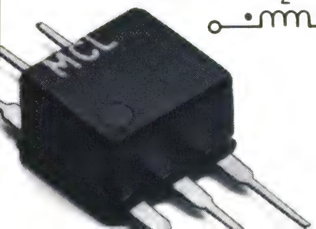
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS			PRICE $
					3dB MHz	2dB MHz	1dB MHz	Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



■ Denotes 75 ohm models

* FOR A AND B CONFIGURATIONS

Maximum Amplitude Unbalance
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range

CIRCLE NO. 50

C72-2 REV. B

WE APPROACH THE MEMORY BUSINESS FROM ONE POINT OF VIEW...

YOURS.

Component Product Family	Memory Size (Total)	Org. (Bits)	Speed (ns)	Package						Special Features	Availability	Military Qualified
				DIP	ZIP	SOJ	PLCC	SOG	PQFP			
SRAMs	1MEG	x1,x4,x8	25-45	X		X				x4 option: OE	Samp: 1H90, Prod: 2H90	Samp: 2H90
	256K	x1,x4,x8	20-35	X	X	X				x4 option: OE	Now	X
	64K	x1,x4,x8	12-25	X		X				x4 options: Separate I/0, OE	Now	X
	16K	x1,x4,x8	12-25	X		X				x4 options: Separate I/0, OE	Now	X
Cache Data SRAMs	144K	x18	20-35				X		X	386/486 Compatible, Fast toe 8ns, Auto write completion, Parity bits	Samp: Now, Prod: 1H90	
	128K	x16	20-35				X		X	386 Compatible, Fast toe 8ns	Now	
SRAMs with Address Latch	16K	x8	100	X		X				Intel 8051 and 8096 compatible	Samp: Now, Prod: 1H90	X
	16K	x8	15-35	X		X				Compatible with high end micro controllers	Samp: Now, Prod: 1H90	X
FIFOs	36K	4Kx9	20-35	X			X			Family options: 300 mil DIP package, Programmable flags, Mailbox register, x16/18, 16 to 18	Samp: 2H90	
	18K	2Kx9	20-35	X			X				Samp: 2H90	
	9K	1Kx9	20-35	X			X				Samp: 2H90	
	4.5K	512x9	20-35	X			X				Samp: 2H90	
DRAMs	4MEG	x1,x4,x16	60-100	X	X	X		X		x4 option: Write per bit	x1,x4 Samp: 1H90, Prod: 2H90; x16: 1991	
	1MEG	x1,x4,x16	70-120	X	X	X	X	X		x16 options: Byte and/or masked write	x1, x4: Now; x16: 1H90	X
	256K	x1,x4	80-120	X	X	X	X				Now	X
	64K	x1	100-150	X			X				Now	X
Quad CAS DRAM	1MEG	x4	70-100			X				Separate CAS control for each DQ input/output	Samp: 1H90, Prod: 2H90	
Pseudo Static DRAM	1MEG	x8	80-120	X		X		X		Unmultiplexed addresses, Simple refresh control	Samp: 1H90, Prod: 2H90	
VRAMs	1MEG	x4,x8	80-120	X	X	X				CMOS, Fully static SAM, Block write, Split read transfer	Samp: 1H90, Prod: 2H90	Samp: 2H90
	256K	x4	100-150	X	X	X				CMOS, Fully static SAM, Serial input	Now	X

Module Product Family*	Word Size (Words)	Org. (Bits)	Speed (ns)	Package						Special Features	Availability	Military Qualified
				DIP	ZIP	SIP	SIMM					
SRAM Modules	256K,64K,16K	x32	15-45		X					Industry standard pin-out with OE	16K, 64K: Now; 256K: 2H90	
	256K,64K,32K	x16	30-45	X						Industry standard pin-out with OE	32K, 64K: Now; 256K: 2H90	
	128K	x8	30-45	X						Compatible with 1MEG monolithic	Now	
DRAM Modules	2MEG,1MEG, 512K,256K	x36	70-120		X		X			Industry standard pin-out	256K, 512K: Now; 1MEG, 2MEG Samp: 2H90	
	4MEG,1MEG, 256K	x9	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
	4MEG,1MEG, 256K	x8	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
	256K	x5	100-120			X				Industry standard pin-out	Now	
	256K	x4	100-120			X				Industry standard pin-out	Now	

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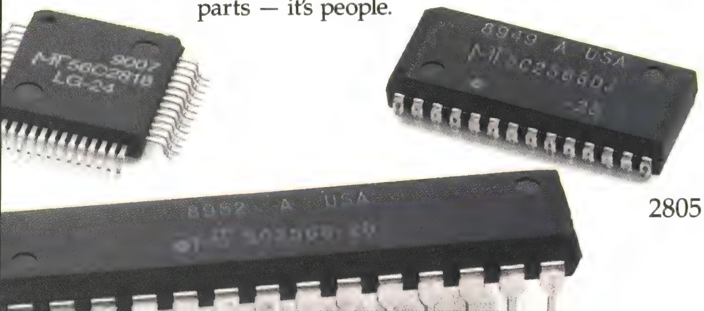

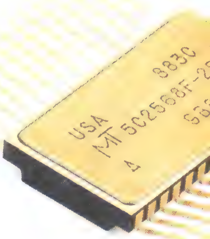

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EDITORIAL

Nix broadcast HDTV

Discussions of high-definition television (HDTV) revolve around two main technologies. First, there's the high-resolution-display technology that you find in flat-panel and cathode-ray-tube (CRT) devices. Second, there's the transmission technology that compresses and expands high-resolution video information. It's this second technology that concerns me. Most people think HDTV signals must fit within existing 6-MHz broadcast-TV channels for HDTV to be a success. They're wrong.

The future of HDTV depends more on the widespread use of fiber-optic technology than it does on adopting signal-compression and -expansion algorithms and standards. For a new technology such as HDTV to take hold, it must offer a 10-fold increase in benefits over the technology it will replace. Broadcast HDTV holds no such promise because tomorrow there will be little to watch but high-resolution versions of today's vacuous programs.

Fiber-optic technology can expand the diversity of communications between a user and a source. And therein lie the keys to HDTV's success—2-way communications and a large bandwidth for a variety of signals. The promise of HDTV is not in higher-resolution TV shows. It's in the ability to communicate a great deal of detailed visual information that might be otherwise inaccessible. A fiber-optic communication network lets us access remote information services; broadcast HDTV offers nothing similar.

Although the potential of fiber-optic communication is great, at today's costs fiber optics won't penetrate most homes. So what will spur the use of fiber optics for 2-way communication, TV, and HDTV? Many legislators and government officials think that a consortium of IC, display, and communications-technology suppliers is the best hope for spurring HDTV development, but they are wrong. The best way is to let the market take its own course. For example, Bell Communications Research Inc recently started transmitting networks' live TV programs through its fiber-optic network. We wish the test success.

Pushing fiber-optic technology into our homes also requires a free-market push from the US government. The Federal Communications Commission must simply say that broadcast-TV channels may not be the best nor the highest use for the spectrum they now occupy. Today, TV channels occupy a 413-MHz portion of the RF spectrum. We could make better use of those sections of the spectrum by auctioning them off to fill highest-and-best-use communication needs. A network may opt to lease a channel or two, but market pressures will push more TV—and future HDTV—stations onto fiber-optic cable.

You can take a nationalistic approach to fiber-optic-based HDTV, too. Often we hear that our Japanese counterparts are ahead in the race for commercial broadcast-HDTV products. Using fiber optics to distribute HDTV signals and to communicate with users favors the electronics industries in which the US leads—workstations, microprocessors, software, and computers, among others. Instead of competing in a race that favors stop-gap broadcasting technologies, let's get a head start in communications technology by "wiring up" with fiber-optic cables now.

Jon Titus

Jon Titus
Editor

Jesse H Neal
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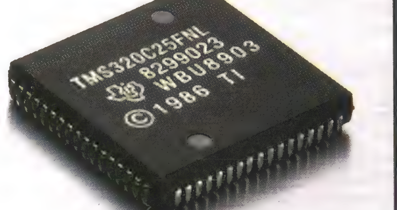

The TMS320C25

- The TMS320C25 takes more than three times as long to compute the same size FFT, while it devours over 47k bytes of memory.[1]
- The TMS320C25 is limited to one access of external data every two cycles.
- The only zero-overhead loop the TMS320C25 can execute is one instruction repeated no more than 256 times.
- Circular buffers? The TMS320C25 doesn't support them.
- The TMS320C25 is programmed with 133 mnemonics like SPAC, BGEZ, MACD, XORX, and SBRK. A multiplication/accumulation is coded as MACD >FF03,*–. While this might not scare the XORX out of you, it's not the easiest thing to debug or maintain.

We're not saying the TMS320C25 is slow. But even if it were twice as efficient as it is now, it'd still be a lot slower at DSP than the ADSP-2100. The fact is, the ADSP-2100 is out in front of the TMS320C25 in performance, readability of code, and development tools.

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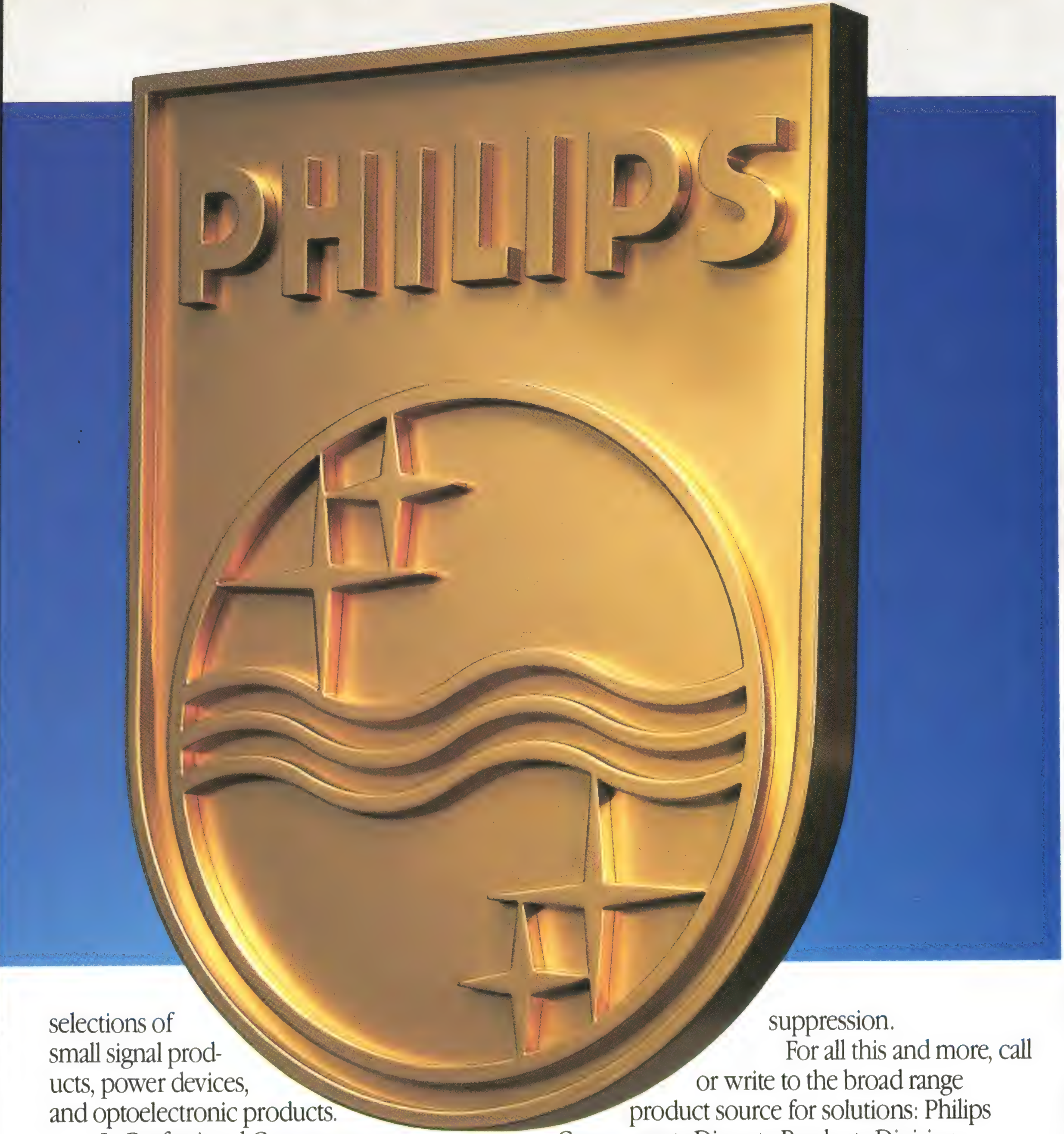
[1] EDN, "EDN's DSP Benchmarks," September 29, 1988.



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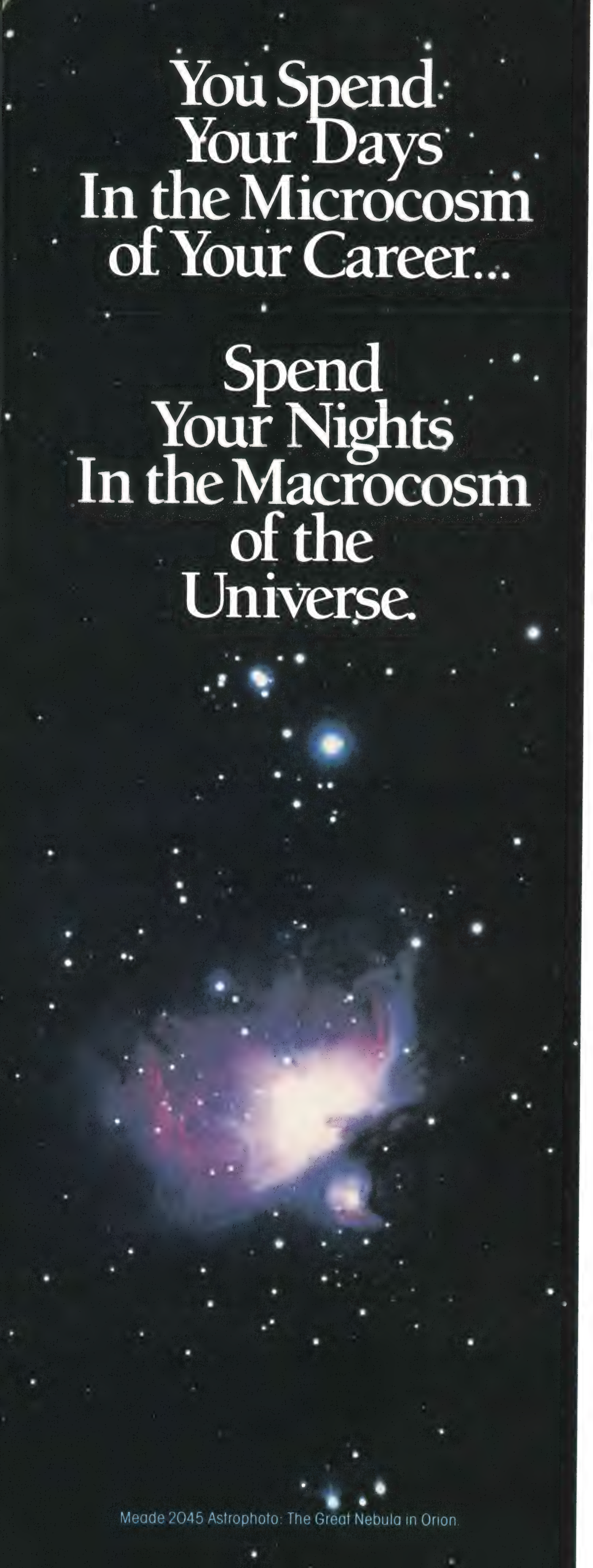
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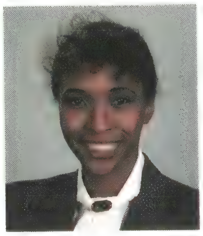
MCA and EISA square off



Two 32-bit bus architectures are vying for your next board design.

J D Mosley,
Regional Editor

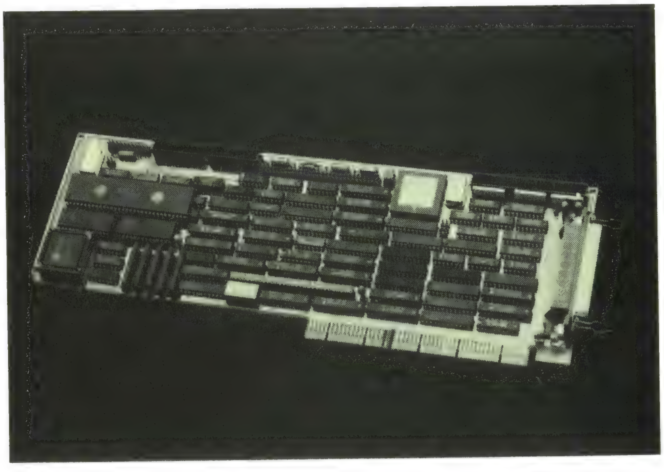
Formal debates, choreographed press conferences, firm stands, and frantic repositioning have characterized the latest small-computer marketing conflict. Both the proponents of the Micro Channel Architecture (MCA) and those of the Extended Industry Standard Architecture (EISA) have taken hostages from the community of plug-in-board manufacturers. However, many board developers have declared this battle of the buses to be a win/win situation: They've hedged their bets by designing products for both bus specifications.

When IBM first announced the Micro Channel Architecture in 1987 with the introduction of its PS/2 line of computers, the company specified 32-bit-wide data-transfer paths and a 20M-byte/sec throughput. A 32-bit PS/2 computer can address as much as 4G bytes of RAM. The spec also eliminated DIP switches and jumpers on plug-in boards by establishing programmable-option-select (POS) registers for automatic system configuration. Each board manufactured for MCA receives an identification code from IBM. A configuration utility compiles this information and automatically assigns addresses and interrupt levels to the board. In addition, as many as seven intelligent plug-in cards, which the company calls bus masters, can assume control of the bus, thus relieving the host CPU of one more set of housekeeping tasks.

An arbitration scheme based on preassigned priority levels for each board helps the MCA central arbitration control point respond to requests for control from bus masters. To prevent any single board from hogging the bus, MCA includes an optional programmable fairness feature, which prevents a board controlling the bus from competing with other boards in the next arbitration cycle. These cycles occur between data transfers and, therefore, use some of the bus bandwidth during arbitration.

IBM keeps prospective PS/2 clone makers at bay by imposing licensing fees for use of the MCA bus. These fees include payment of a percentage of the developer's revenues as well as a retroactive fee for presumed past bus-license infringements.

In protest, the Gang of Nine—with Compaq leading the revolt—proposed



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an alternate architecture. (The other gang members were AST Research (Irvine, CA), Epson (Torrance, CA), Hewlett-Packard, NEC Information Systems Inc (Boxborough, MA), Olivetti (Somerville, MA), Tandy Corp (Fort Worth, TX), Wyse Technology (San Jose, CA), and Zenith Data Systems (Glenview, IL).) They proposed an extension of the Industry Standard Architecture (ISA), which every clone maker had become intimately familiar with due to the popularity of IBM PC/AT and compatible computers. They dubbed this new architecture the Extended Industry Standard Architecture (EISA). Like MCA, EISA provides for bus masters and 32-bit-wide data communications. But the EISA spec further provides for a maximum throughput of 33M bytes/sec in burst mode (versus MCA's 20M-byte/sec burst-mode throughput), a 58-in.^{2} expansion-card size (versus MCA's 36-in.^{2} size), and 4.5A per plug-in-board slot (versus MCA's 1.6A allotment per slot). **Table 1** compares these and other MCA and EISA specifications.

In addition, EISA's bus-master arbitration scheme uses a central arbitration controller that grants bus ownership on a rotational basis. Unlike MCA's arbitration scheme, EISA's uses none of the bus's data-transfer bandwidth because arbitration occurs in parallel with other bus activity.

To its credit, the MCA plug-in board connector offers electromagnetic performance superior to that of ISA's connector because a ground pin lies between every four signal pins. To improve the poor electromagnetic characteristics of its ISA roots, the EISA board connector has 17 ground pins interspersed among the ISA signal pins.

In response to EISA's superior specs, last October IBM announced future MCA capabilities that will include 64-bit streaming data procedures (SDP) for an 80M-byte/sec data-transfer rate, improved fault detection, data- and address-parity checking, and a software protocol for improving bus-control communication among expansion cards and the main CPU. A proposed synchronous channel check would isolate a fault to a particular device and then disable that device without crashing the system.

IBM also proposed future MCA extensions that would double the bus's data-transfer rate to 50 nsec or less. If IBM does implement these extensions, the top data-transfer rate with SDP would be 160M bytes/sec. Of course, EISA devotees note that IBM has merely voiced speculations and has not implemented any of these proposed improvements. Yet, because IBM alone controls developments in the MCA spec, the company can rapidly enact future improvements and is limited only by the available technology. In contrast, EISA was specified by committee and already pushes the technical limits for improvements while maintaining compatibility with its ISA predecessor.

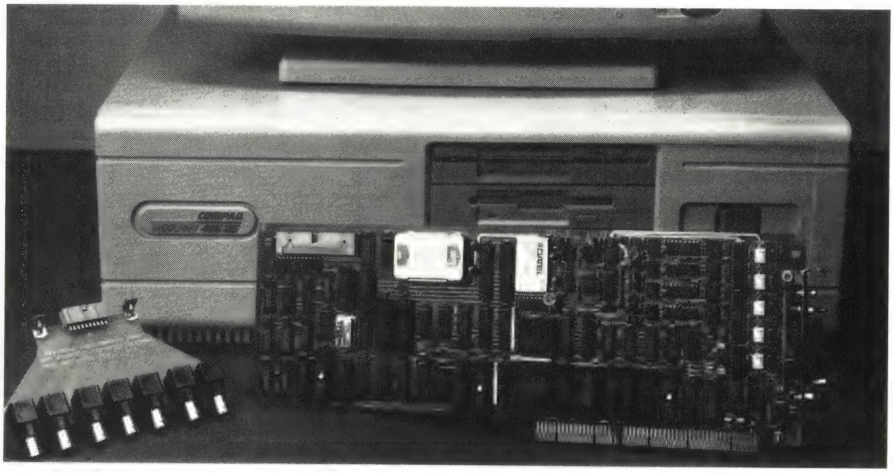
Table 1—Comparison of MCA and EISA specifications

Specification	MCA	EISA
Compatibility	Not ISA compatible	ISA (PC/AT) compatible
Bus size		
Bus size	16 or 32 bits	32 bits
Memory address space	4G bytes (32 bits) 16M bytes (24 bits)	4G bytes (32 bits)
Bus clock	10 MHz	8.33 MHz
Bus transfers		
Speed		
Memory cycles	20M bytes/sec	33M bytes/sec
I/O cycles	20M bytes/sec	22M bytes/sec
Single-cycle burst transfers	No	Yes
Transfer timing	Asynchronous	Synchronous
Bus-master support		
Number supported	7	6
Arbitration	Distributed in series	Centralized in parallel
Priority	Prioritized at system start-up (optional fairness)	Equal and fair
DMA controller		
Number of channels	8	7
Data size	16 bits	32 bits
Max DMA transfer speed	5M bytes/sec	33M bytes/sec
Transfer type	Fetch and deposit (serial)	Fly by (parallel)
Interrupts		
Number of lines	11	12
Type	Level	Edge or level
System configuration		
Automated	Yes	Yes
Nonvolatile-RAM storage of system configuration	Yes	Yes
Expansion-board configuration	Programmable	Programmable or switches and jumpers
Slot-specific addressing	Yes	Yes
Bus translation	No	Yes
Mechanical/power		
Board size	36 in.^{2}	58 in.^{2}
Connector	58 or 89 pins 0.05-in. centers Edge Single height	188 pins 0.05-in. centers Edge Double height
Connector grounding	Grounds for every four signals	EISA pins intersperse grounds between old ISA pins
Board power	1.6A at 5V	4.5A at 5V

(Table courtesy National Instruments Corp)

MCA and EISA plug-in boards

However, there's good news from the EISA consortium for board developers: You no longer have to fork over $2500 and sign a nondisclosure agreement to get a copy of the EISA spec, although it's still not available for free. BCPR Services (Washington, DC), which controls distribution of the spec, charges $125 for printing you a copy. For $450, BCPR will print you one copy, grant you the right to make five copies of your copy, provide a year of updates to the spec, give you access to the EISA Forum Electronic Bulletin Board, and let you purchase additional copies of the spec for $100 apiece. The EISA spec details the physical and electrical requirements for I/O lines, connectors, and timing logic. Call BCPR at (202) 371-5921 to request a free information kit, which contains a technical synopsis of the spec.



This EISA card can sample analog signals at rates reaching 1M sample/sec with 12-bit resolution. *The EISA-A2000 from National Instruments has four simultaneously sampled analog input channels with analog and digital triggering for the high-speed level and phase analysis of multiple waveforms.*

So, which bus should you design your next circuit around? Jerry Roby, president of IMC Networks Corp, says his company began developing its latest Ethernet adapter for the MCA bus simply because IBM PS/2s have been available for two years. Compaq didn't roll out its SystemPro line of EISA computers until November of last year. It's interesting to note that every currently available EISA host com-

Table 2—Representative MCA and EISA plug-in boards

Manufacturer	Model	Bus	Board description	Price	Bits	Bus master
Adaptec	AHA-1640	MCA	SCSI host adapter	$283	16	Yes
	ACB-2610	MCA	ST412/506 MFM hard-disk controller	$135	16	No
	ACB-2670	MCA	ST412/506 2, 7 RLL hard-disk controller	$165	16	No
Codenoll Technology	CodeNet 8300	EISA	Fiber-optic Ethernet adapter	$995	32	Yes
	CodeNet 9500	EISA	FDDI adapter	$6695	32	Yes
Computone	ALC Communications Controller	EISA	I/O communications controller	$1595	32	Yes
Comtrol	Hostess 550/MC	MCA	Buffered I/O communications controller	$745	16	No
	Ultra 186/MC	MCA	Intellligent I/O communications controller	$1295	16	No
Digiboard	DigiChannel C/X	EISA	Cluster communications controller	$2195	32	No
IBM	PS/2 Wizard Adapter	MCA	Application accelerator	$7000	32	Yes
IMC Networks	PCnic EISAbus	EISA	Ethernet adapter	$1295	32	Yes
	PCnic MCAbus	MCA	Ethernet adapter	$995	32	Yes
Interphase	E/SCSI 4810 Barracuda	EISA	SCSI adapter	$2490	32	No
Madge Networks	Smart 16/4 EISA Ringnode	EISA	Token-ring adapter	$1495	32	Yes
Matrox	Illuminator 16/MC	MCA	Video-graphics controller	$1795	16	No
	MP-860	EISA	Scalable parallel processor	$6300	32	Yes
Mylex	LNE 390A	EISA	Ethernet adapter	$425	32	No
	DCE 376	EISA	SCSI host adapter	$1700	32	Yes
	GXE 020A	EISA	High-resolution graphics adapter	$5100	32	Yes
National Instruments	EISA-A2000	EISA	1M-sample/sec data-acquisition board	$2995	16	No
Newport Systems Solutions	WNIC-MCA	MCA	Wide-area-network interface coprocessor	$1295	16	No
Novell	NE3200	EISA	Ethernet adapter	$1295	32	Yes
Proteon	ProNET-4/16 EISA	EISA	Token-ring adapter	$1195	32	Yes
Standard Microsystems	ARCnet-EISA3200	EISA	ARCnet adapter	$995	32	Yes
Ultrastor	Ultra 22 EISA	EISA	ESDI controller	$550	32	Yes
VideoLogic	DVA-4000/MCA	MCA	Full-motion digital video adapter	$2495	16	No

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puter costs more than $10,000, whereas IBM offers a Model 30 PS/2 for a base price of $2255.

Audrey Harvey, engineering manager of the data-acquisition division of National Instruments, points to EISA's present technical superiority as the basis for her company's decision to eschew MCA. Harvey maintains that EISA's 32-bit DMA controller and higher bus-transfer rates permit it to outperform MCA. The 33M-byte/sec transfer rate of the EISA bus is immediately available via Intel's EISA chip set; MCA will be limited to 5M-byte/sec transfers until faster DMA chips arrive.

With respect to MCA, Harvey says that the spec's significantly smaller board size, current limitations, and complex arbitration logic represent significant restrictions for board designers. Furthermore, she notes that when using an EISA-based computer, you can rewrite the DMA-driver software for an existing 16-bit ISA board. Thus, you can make ISA boards operate at the 4M-byte/sec data-transfer rate. EISA provides bus translation via the system board, thus making it easy for a 32-bit EISA bus master to access a board with a different data-bus width—even if that slave is an 8- or 16-bit ISA board.

Such backward compatibility was the original hue and cry of the Gang of Nine. And although MCA advocates scoff at the notion that an end

For more information . . .

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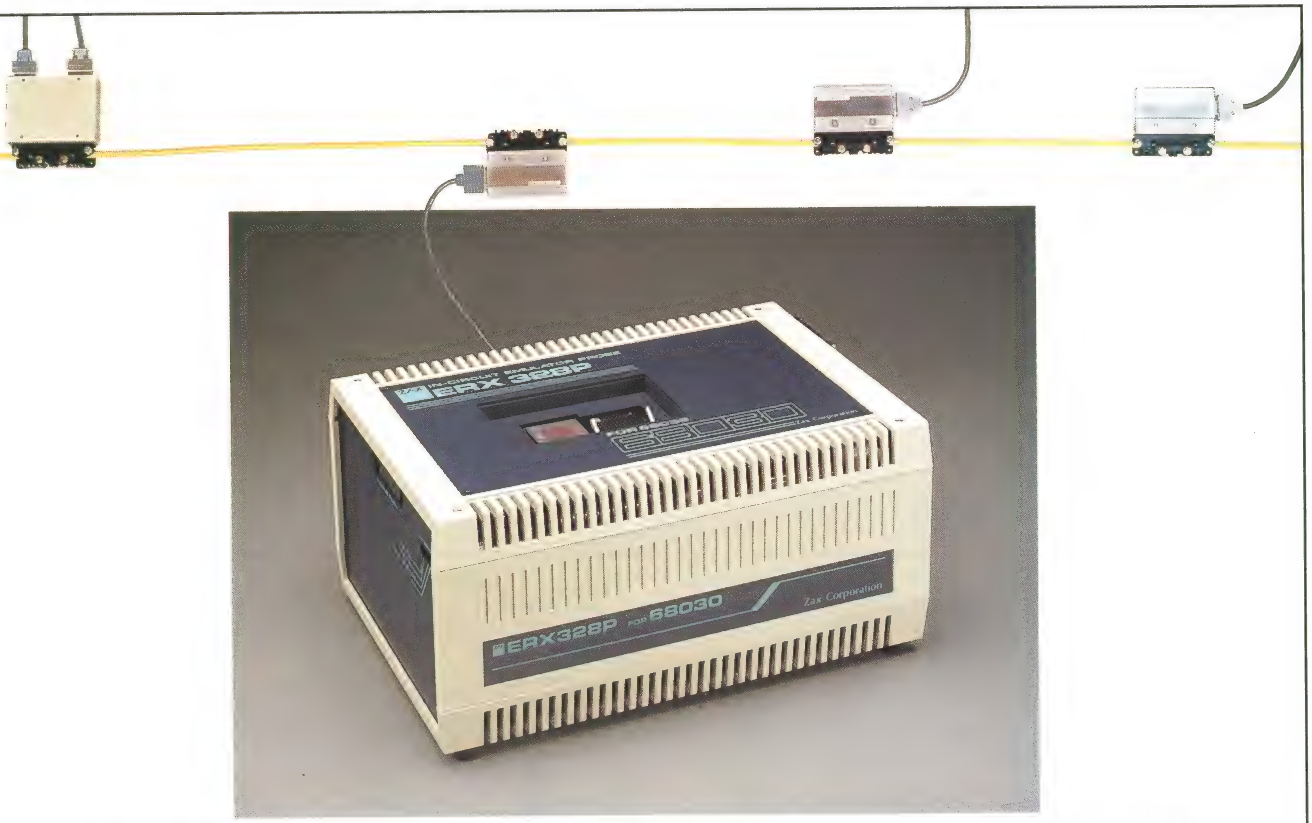

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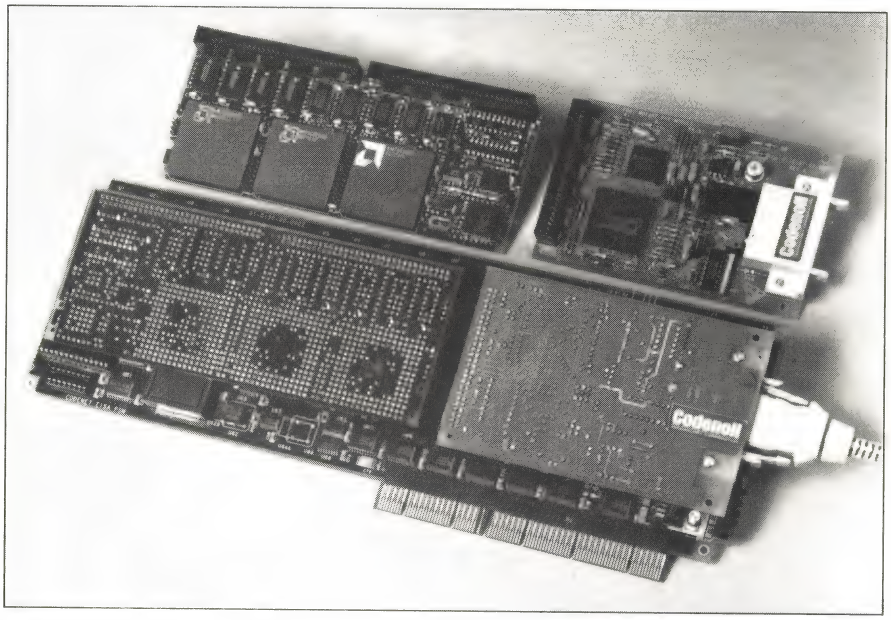

***The CodeNet 9500 EISA/FDDI Network board uses modular daughter boards** to provide easy upgrades. The Codenoll Technology Corp board facilitates FDDI's 100M-bps data-transfer rates and takes advantage of EISA's wide bus bandwidth.*

user would purchase a $20,000 Compaq SystemPro to pack it with cards from an old IBM PC/XT, the fact remains that thousands of plug-in cards are currently available for EISA bus-based computers, thanks to the computers' ability to use ISA cards. If you buy a SystemPro today, you won't have to wait for some manufacturer to market a bus-master modem card with automatic configuration before you can tap into CompuServe. You'll be able to immediately enjoy the low prices that the mature ISA market offers.

Unfortunately, implementing the bus-master capability has proven to be the major stumbling block as plug-in-board manufacturers race to market with their offerings. Bugs delayed the planned third-quarter-1989 availability of Intel's 82355 Bus Master Integrated Circuit (BMIC) for the EISA bus. The BMIC provides an interface between a plug-in card's local functions and the EISA bus's master protocol by arbitrating bus ownership. The BMIC is available in sample quantities for $35. Robert Neilley, director of marketing communications at Codenoll Technology, states that the bus-master concept is complex and notes that the BMIC—a single chip—only has about 16 nsec to grab control of the bus, manipulate its speed and traffic, and then relinquish control.

Pitfalls abound for all

Even IBM failed to meet its announced December 1989 shipping date for its PS/2 Wizard Adapter. Jointly developed by IBM and Intel, the Wizard is a $7000 MCA bus master card with a 33-MHz, 64-bit i860 μP. This 1,000,000-transistor chip calculates at speeds reaching 64M flops and 27 MIPS. It contains a RISC (reduced-instruction-set computer) integer core, a floating-point processor, a graphics unit, and internal instruction and data caches.

Louis Regniere, project director for Matrox Electronic Systems' parallel-processing group, notes that although the Wizard is a single-slot board, you have to leave the slot next to it empty because the Wizard consumes more than its MCA-allotted 1.6A. Despite this slip in IBM's plans, more than 1000 MCA bus boards are available, and at least 15 provide bus-master capability.

Several other plug-in-board manufacturers planned first-quarter-1990 announcements for MCA-or EISA-based products, but production bugs caused them to delay their announcements until later in the year. Other manufacturers have refused to commit resources to further technical development until the EISA and MCA bus specifications stabilize. Several companies assert that they're still finalizing the development path their products will follow. Regardless, all board manufacturers agree that 1990 will be a prolific announcement year for EISA and MCA bus-master boards and other products.

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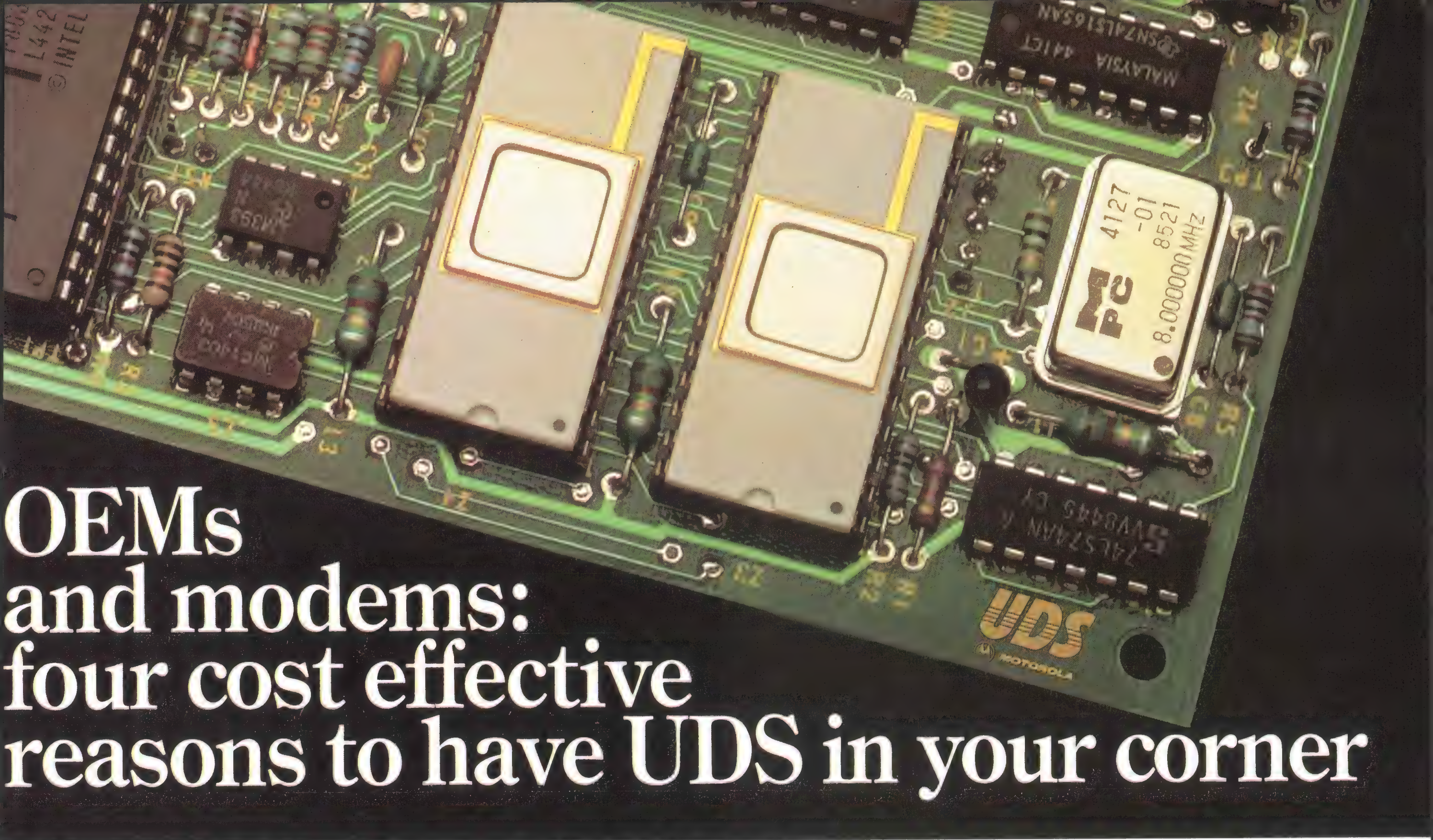

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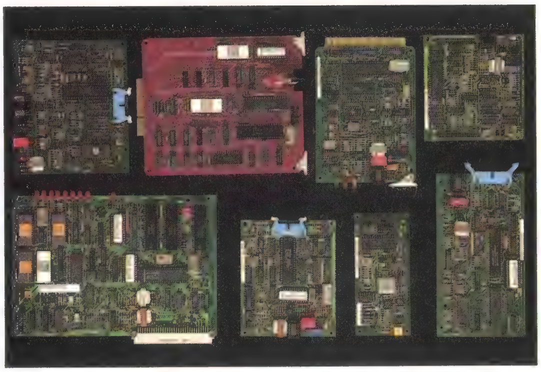

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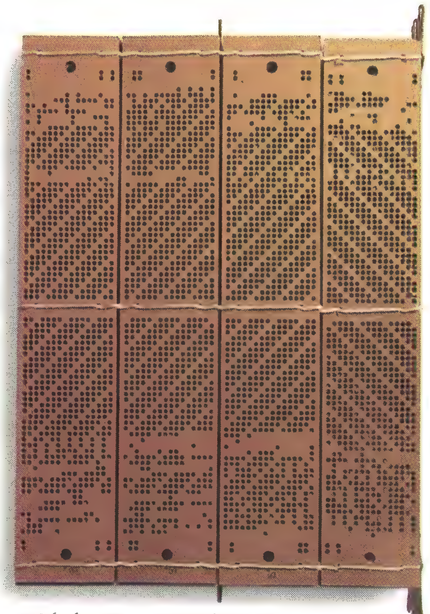

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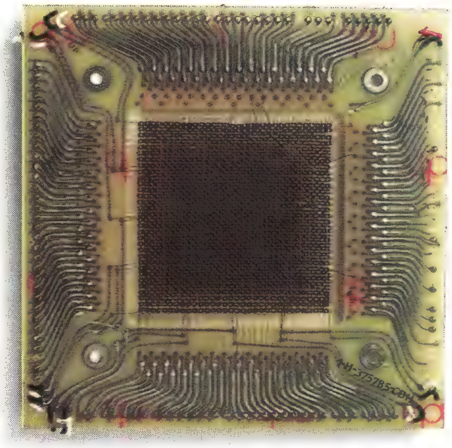

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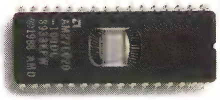

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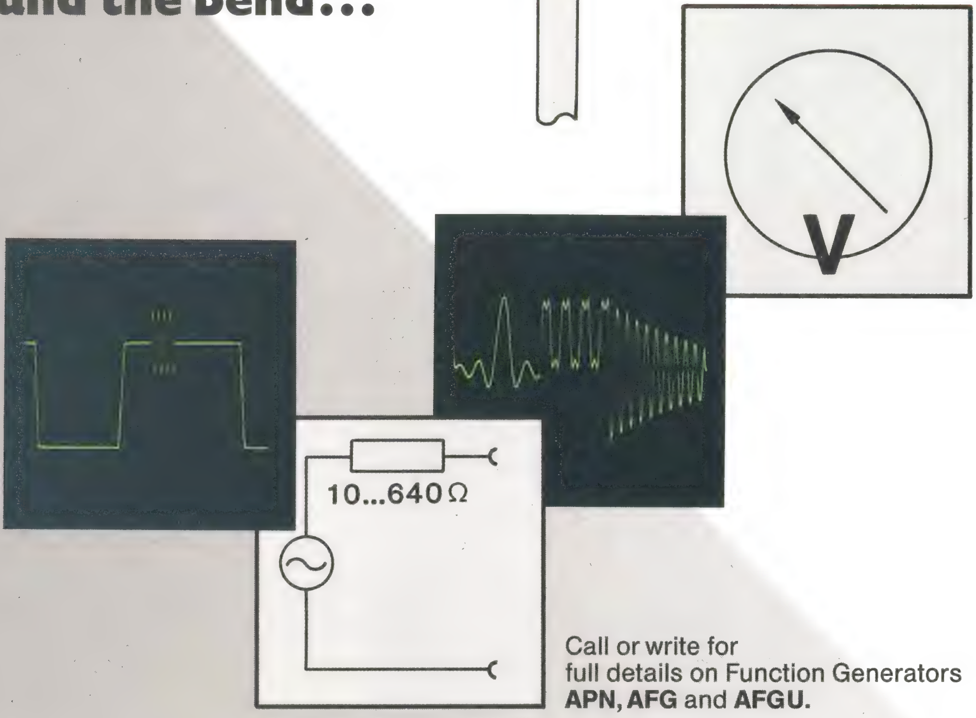

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16-bit debugging tools perform at low cost

When budgets are tight, low-cost debugging tools may be the only option. Fortunately, these tools are versatile enough to perform many tasks.

Richard A Quinnell,
Regional Editor

A favorite way for budget-conscious managers to control project costs is to disapprove the purchase of expensive (>$10,000) test equipment, such as processor-specific debugging tools. Lower-cost (<$6500) alternatives can satisfy many applications and may be the best choice for your tight budget—if you can live within their limitations.

When discussing debugging tools, most design engineers think of in-circuit emulators, powerful devices that are becoming increasingly expensive. The continual rise in processor clock rates is forcing emulator designers to use more expensive memory and logic. At the same time, the proliferation of processor variants is reducing the number of customers using each type of processor, so emulator vendors must charge more per unit to recover their development costs.

The higher-priced emulators are designed to tackle the toughest problems in the fastest systems. However, less capable, lower-cost tools can handle many software-debugging problems. After all, there's no sense in buying a Porsche if all you need to do is drive around town.

The lower-cost tools are most useful when your target hardware is at least 90% functional and doesn't need to run at state-of-the-art speeds. With a relatively stable hardware platform, debugging activity can center on the software. The more functional your software is, the cheaper the tool you can use.

The cheapest development tool is probably a monitor program that resides in ROM on your system and talks to a dumb terminal. This time-honored helpmate has been around as long as the microprocessor and is quite useful for handling small debugging problems and assembly-language patches of a few dozen lines. You can tackle larger debugging problems using just a monitor, but it's a tedious task.

A typical monitor program lets you examine and change memory and registers, set software breakpoints, and begin the execution of code at any location. Many of these programs include limited

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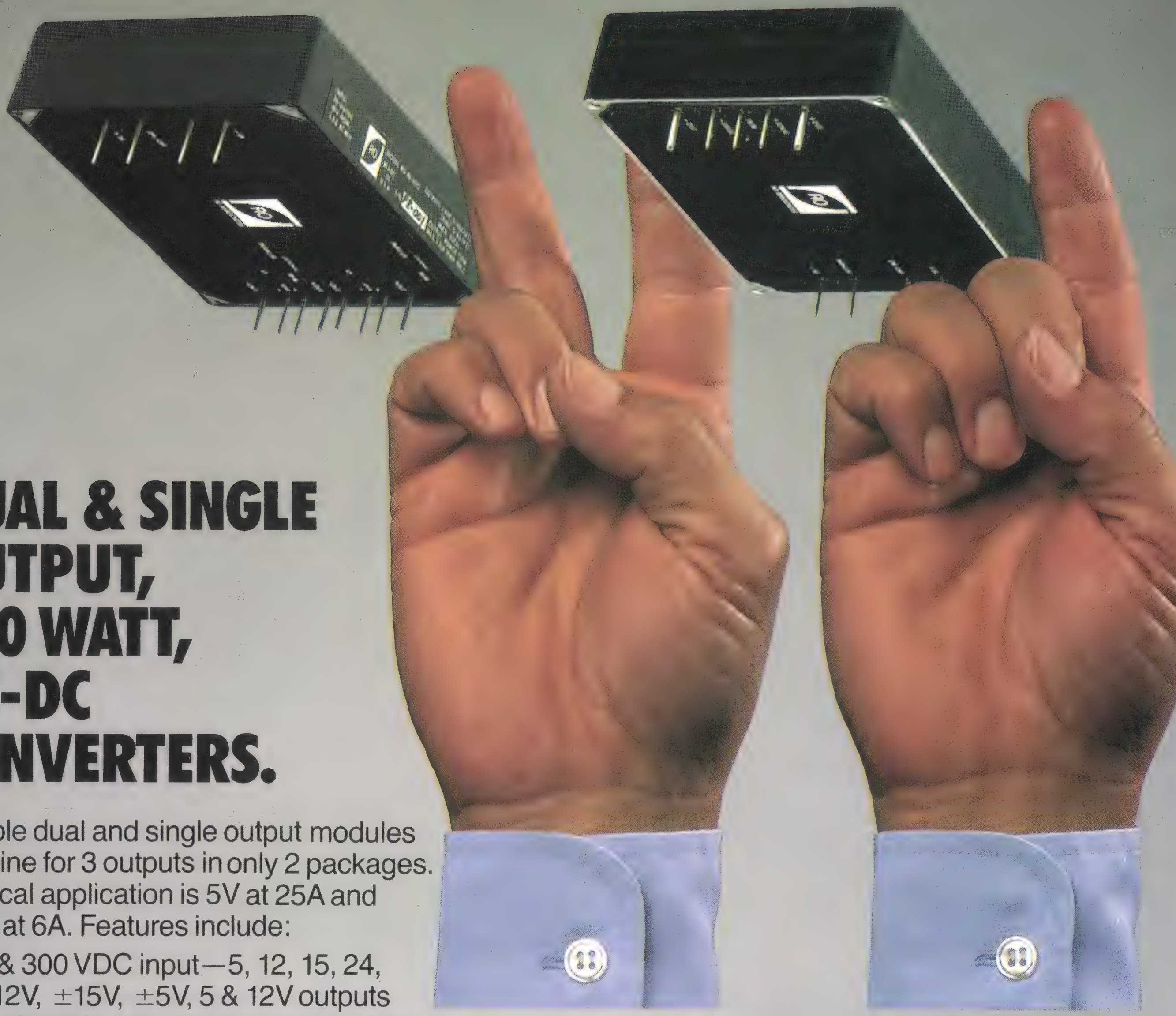

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line assemblers and disassemblers.

Through clever and patient use of the monitor, you can check the operation of any peripheral in your system and test I/O ports and memory. You can also run your software at full speed on the target system, halting the processor to see if the software is behaving. If it's not, you can isolate the problem by using a lot of intuition—that is, guessing where the mishap has occurred and putting in breakpoints to verify your guess.

Almost every processor vendor offers a monitor program for its products. Vendors usually include monitors as part of a development or evaluation board, but you may be able to buy them separately. For example, Zilog (Campbell, CA) offers monitor source code for its entire processor family. The source code lets you easily adapt the monitor to your system's configuration. Development boards with monitors typically cost a few hundred dollars. Motorola (Austin, TX) and National Semiconductor (Santa Clara, CA) also offer development boards.

Simple monitor programs have a number of obvious limitations. Their communications with the user are typically slow and cryptic, comprising ASCII characters flowing along a serial data link. The monitor requires a serial I/O port for communications. Further, your system must use RAM instead of ROM so you can set breakpoints in executable code.

The monitor-based debugger is a giant step above the basic monitor. The debugger is actually two pieces of software. One is a monitor program that resides in your system's memory; the other runs on a host computer. You interact with the program in the host computer, which in turn uses the monitor to control the target system.

The Xray debugger from Microtec Research is an example of a monitor-based debugger. It works with the 680x0 and 80x86 families of processors and comes in versions that run on IBM PC-compatible computers, VAXes, or on Sun, HP, or Apollo workstations.

Depending on your board's capabilities, the debugger communicates to the monitor program on your board through an RS-232C link, a SCSI port, or Ethernet. The monitor program occupies approximately 5k bytes of memory and is locatable anywhere within your system's memory. A PC-based Xray debugger with a monitor starts at $2000. Add Microtec's C compiler and you've turned your PC into a complete development system for around $5000.

Other monitor-based debuggers come from Intermetrics and First Systems. Intermetrics' RMXDB handles the 68000 and 8086 families as well as the 68332. The debugger

Avoid nasty surprises: design for your tools

All too often, designers defer the purchase of debugging tools until the need for them is sitting on the bench, malfunctioning. Tools bought in the resulting haste may not work well in the system because of electrical or timing incompatibilities. If you're able to select your tools before you start designing, however, you can take a number of steps to avoid potential problems.

One of the most important steps is to design around each tool's electrical characteristics. Low-cost tools may require access to system resources. Even a state-of-the-art, minimal-impact in-circuit emulator has some effect on the target while it's connected.

Probes add loading effects to the processor output, for example, and cables delay signals between the emulator and target. If you don't account for these effects in your design, your system may crash when the emulator is connected or—even worse—the emulator may mask the problem while it's connected.

If you know your tool's characteristics, you can easily add the proper resources and compensate for timing and loading effects at the design stage. Once your design is in hardware, the task may become unmanageable.

Keep in mind the tool's physical requirements. For example, leave enough room on your board to accommodate your tool's probe. Also, choose the processor's location in your system carefully. If it's buried too deeply, your probe cable might not be able to reach it. Nothing is more irritating than having a debugging tool you can't use because you can't attach it properly to your target.

Make sure that all your development tools—emulator, compiler, linker, and debugger—work well together. Many tools offer source-level and symbolic debugging, but only if your compiler provides the necessary symbol information. Of course, you can ensure compatibility by purchasing a tool suite from one manufacturer. If you already have the code-generating tools, however, and you're simply adding debuggers to your kit, be sure to test the two together.

costs $4050 with a C compiler. The First Systems Microscope debugger for the 80x86 and V Series processors costs $2780. Its monitor portion requires only 1700 bytes of ROM.

High-level user interface

Because it runs on a host computer, a monitor-based debugger has many advantages over a simple monitor. The most obvious advantage is that the host takes over communications with the monitor, allowing you to use more complex commands. Further, the communications link operates with binary data instead of ASCII, and it provides error checking. The result is faster, more reliable communications with the target.

The host computer provides much more than enhanced communications with the monitor, however—it makes the whole system easier to use. Monitor-based debuggers offer pop-up menus and on-line help messages, and they separate the information into display windows for easier viewing.

If the debugger has access to the source-code files, it will let you work with your code at the source level. However, to provide the debugger with the necessary information for this feature, your compiler must generate the proper files. The Intermetrics RMXDB, for example, works only with the Intermetrics compilers. Microtec's Xray debugger works with C compilers that generate files in Intel's (Santa Clara, CA) output module format (OMF). The First Systems Microscope debugger works with C, Pascal, and Fortran OMF compilers. First Systems also offers a $90 utility program that converts files generated by Microsoft's compilers to the OMF.

One drawback of monitor-based debuggers is their dependence on target resources. If you want to use breakpoints, your code must originate in RAM. You must provide a communications port so the target can talk to the host. In addition, some of the processor's resources are commandeered by the monitor to help it control the processor.

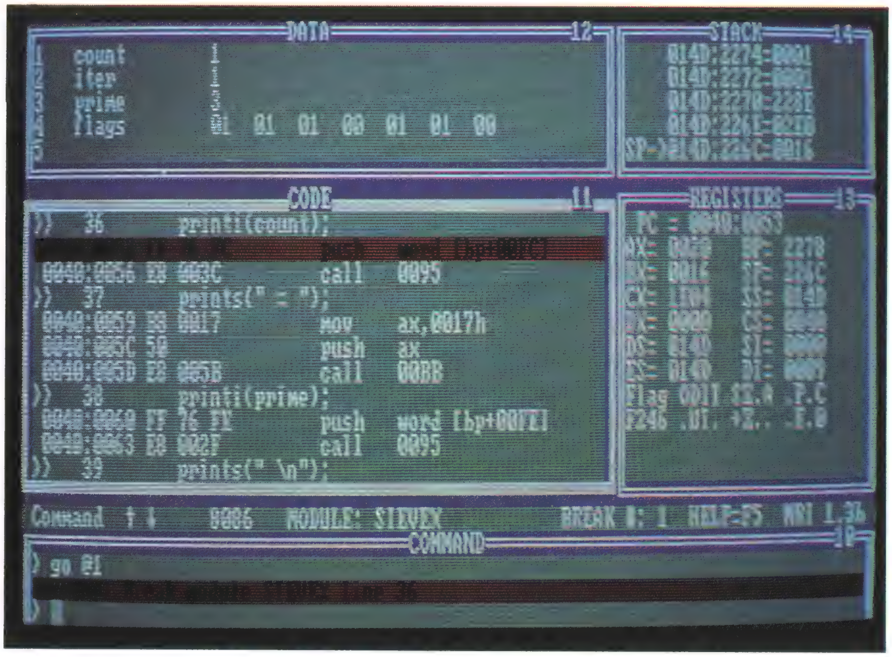
To regain control of the processor while it's executing your code, the monitor program must have a means of altering the program flow. The Microscope debugger, for example, uses interrupt request lines to halt the processor for single-step operation and at breakpoints. The Xray debugger is less intrusive; it uses the processor's illegal instruction and trace vectors to re-enter the monitor.

If you can permanently dedicate board resources for the monitor's use, you'll receive the added benefit of built-in testability. Simply leave the monitor resident on your board when it goes into production (and don't forget to pay any license fees). The monitor will become a tool that the manufacturing and field-service people can use. They may not bless you for your thoughtfulness, but they'll probably stop cursing.

A major limitation of monitor-based debuggers is their inability to provide any runtime trace capability. To see what has happened in your system, the debugger must stop the processor and query its status. To watch your code in operation, you must single-step the processor—a tedious task.

The Intermetrics RMXDB uses single stepping to provide a pseudotrace feature: it's a trace, but it's slow. The debugger steps the processor through your program, keeping a history of the program-counter value in RAM. When you stop the trace, the record allows you to see what the processor actually did.

To acquire real-time trace capability, you'll have to spend a lot more money to acquire a bus monitor/ROM emulator such as the Orion Instruments Unilab 8620 ($6280) or the Softaid IceAlyzer



```
1  count
2  iter
3  prime
4  flags        01  01  01  00  01  01  00
```

```
>>   36        printi(count);
0040:0056 E8 003C          call   0095
>>   37        prints(" = ");
0040:0059 B8 0017          mov    ax,0017h
0040:005C 50               push   ax
0040:005D E8 005B          call   00BB
>>   38        printi(prime);
0040:0060 FF 76 FE         push   word [bp+00FE]
0040:0063 E8 002F          call   0095
>>   39        prints(" \n");
```

```
Command  ↑ ↓    8086   MODULE: SIEVEX           BREAK #: 1  HELP=F5
> go @1
>
```

Even low-cost tools can offer source-level debugging. *By coupling your source code with the compiler's assembly-language product, tools such as the Microtec Xray debugger let you work with both details and abstractions.*

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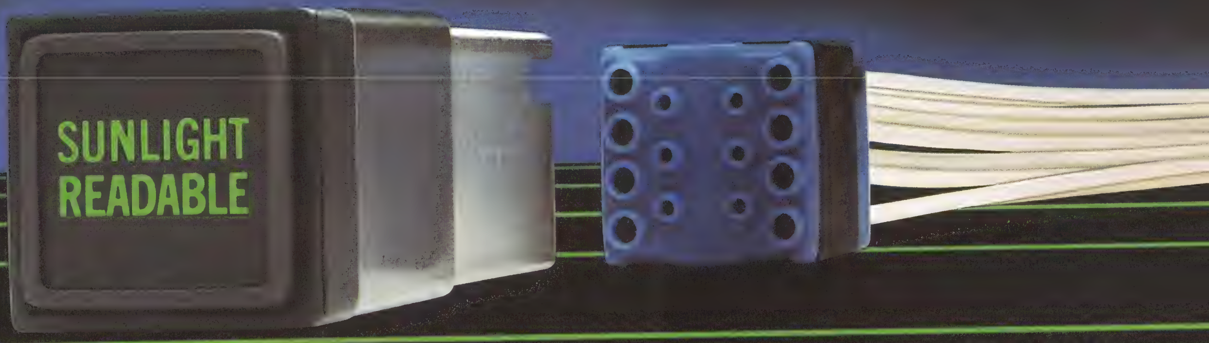

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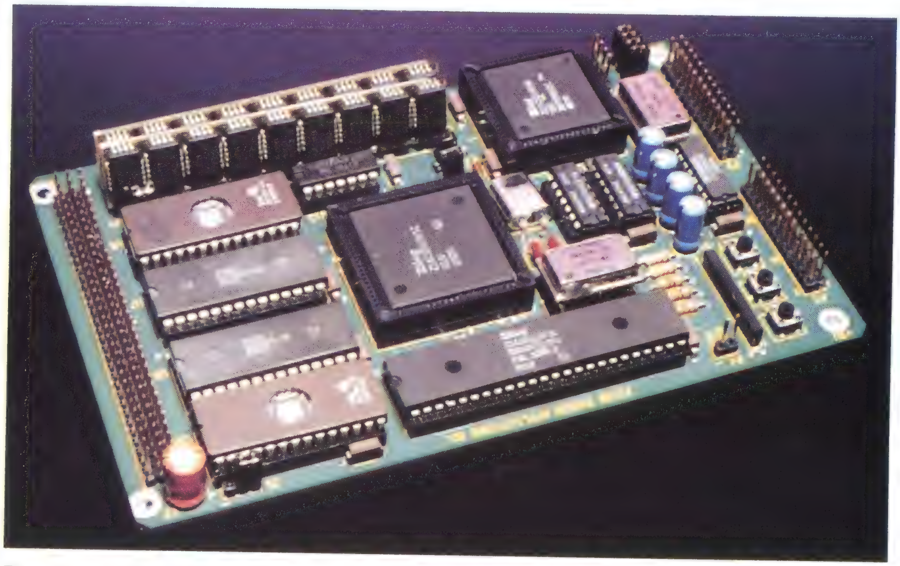
($5280 with source-level debugging). Both units require an IBM PC or compatible host computer. Unilab comes with an add-in card for connection to the host. The IceAlyzer uses a serial communications link.

These emulators connect to the target processor, monitoring address, data, and control signals as the processor executes code. The Unilab can also monitor program execution by plugging into a ROM socket. The bus monitors can acquire and display trace data without halting the processor, because they simply watch rather than control it.

In addition to monitoring processor operation, the units emulate the target's ROM, allowing you to debug your code without relocating it to RAM space. To prevent bus contention, however, you may need to remove or disable the ROM on your target during emulation.

The emulation capability lets the unit control the processor's operation without using any of the system's resources. Because the emulator has complete control of the program memory, it can insert the control software directly into the instruction sequence. The Unilab will also use the processor's nonmaskable interrupt, if available, to provide hardware breakpoints.



Development boards with monitor programs are the least expensive debugging tools. *The boards provide both a stable platform on which to test your code and a window into its operation. Most IC manufacturers offer these boards for a few hundred dollars. (Photo courtesy Zilog Inc)*

For more information . . .

For more information on the debugging tools and processors discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Like the monitor-based debuggers, the emulators use the host computer to provide a variety of useful features, including windowed displays, source-level debugging, and on-line help. In addition, the host computer can keep track of all code-memory access and create a histogram of code usage.

This histogram feature, called a performance analyzer, lets you determine where in your program the processor is spending most of its time. Such sections of code are prime candidates for optimization. You can also find out which sections of code are dead (never executed).

True in-circuit emulation

Even though the Unilab and the IceAlyzer have most of the functions found in in-circuit emulators, they differ in a few critical areas. First of all, the ROM emulators can only see what's happening outside of the processor. To allow you to examine internal registers and eliminate instructions that were fetched but not executed, the ROM emulators model the processor's operation. They keep track of what

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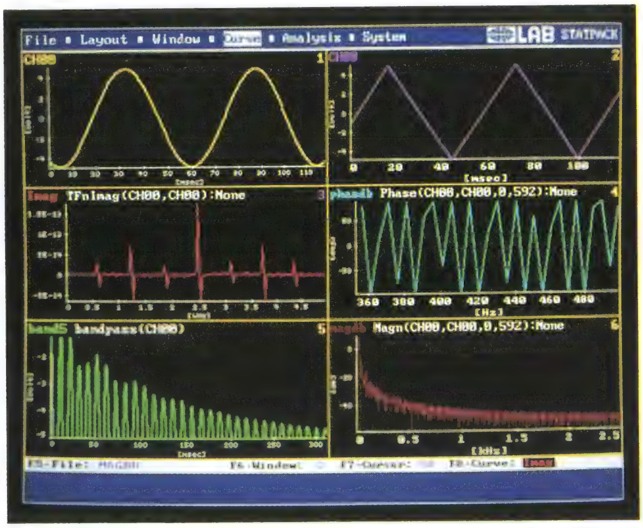

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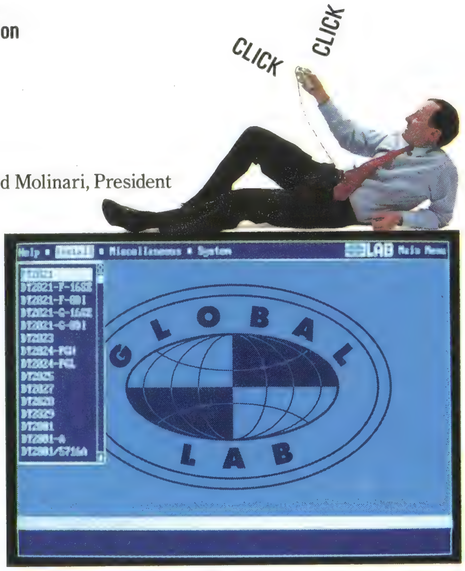

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values the internal registers should have and display those values. In-circuit emulators mimic the processor so that the emulator can directly read all of the processor's internal states.

Another critical difference between ROM emulators and in-circuit emulators is that an in-circuit emulator can prevent the processor's memory-access cycle from appearing at the target and a ROM emulator can't. Thus, an in-circuit emulator can overlay the ROM in your system without causing bus contention.

A third difference between these two types of emulators is their speed. ROM emulators peak at 16 MHz, whereas certain in-circuit emulators can match the highest available processor speeds.

In many development projects, low-cost tools fill the bill most of the time. You may encounter complex problems, however, when the power of a top-notch in-circuit emulator is vital. In that event, you may want to rent the expensive tool. Rental companies such as Leasametrics Inc (Foster City, CA), as well as the manufacturers themselves, offer tools at a monthly rate of 9% to 11% of their price.

If several people are working on development at the same time, you can also try providing a range of tools. Acquire one in-circuit emulator and several debuggers. That way, each person on the team has a debugging tool and can use the "big gun" when necessary. Many debuggers, such as the Intermetrics XDB 5.0 and the First Systems Microscope, can directly control an in-circuit emulator, so you can use it as an extension of the debugger's capability.

Finally, remember that a tool costs more than its price. Carefully examine the warranty and service provisions to be sure you'll have the vendor's full support whenever you need it. EDN

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1. Berger, Arnold S, "Following simple rules lets embedded systems work with µP emulators," *EDN*, April 13, 1989, pg 171.

2. Strassberg, Dan, "ICs and tools tame tough technology," *EDN*, October 26, 1989, pg 73.

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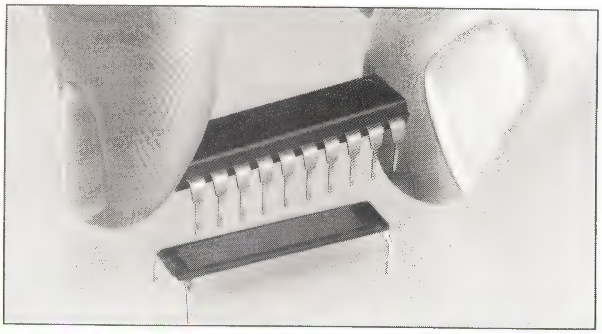

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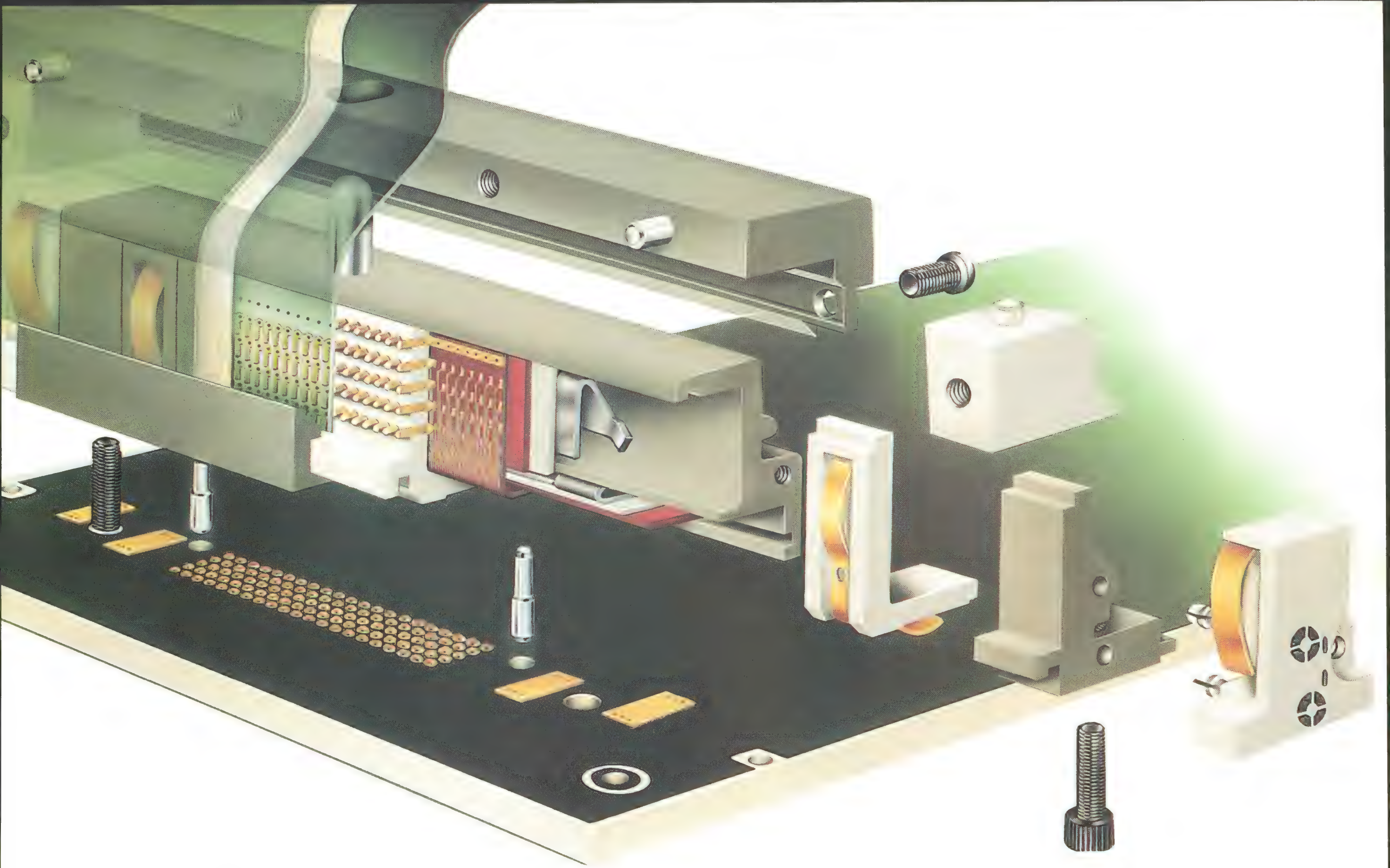

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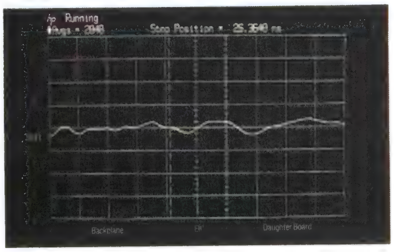

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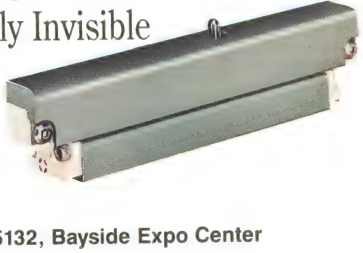

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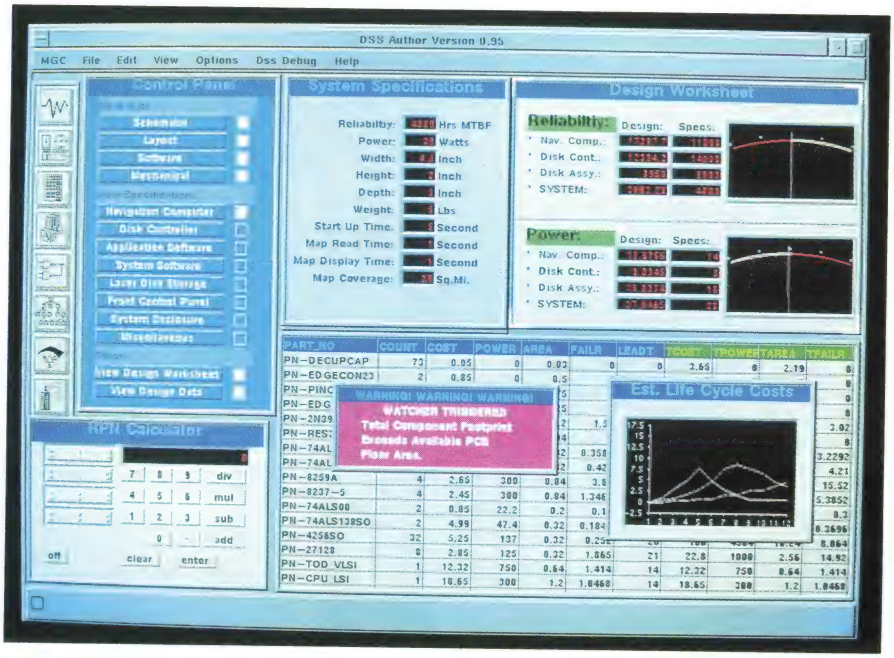

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PN–2N39				2	1.5					3.02
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PN–74AL				2	0.358					3.2292
PN–74AL				2	0.42					4.21
PN–8259A	4	2.65	300	0.84	3.8					15.52
PN–8237–5	4	2.45	300	0.84	1.346					5.3852
PN–74ALS00	2	0.85	22.2	0.2	0.1					0.3
PN–74ALS138SO	2	4.99	47.4	0.32	0.184					0.3696
PN–4256SO	32	5.25	137	0.32	0.25					0.864
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PN–CPU LSI	1	18.65	300	1.2	1.0468	14	18.65	300	1.2	1.0468

***Meters and gauges (top) built into** the Concurrent Design Environment's decision-support system can give you instant feedback on a number of critical project parameters. Software constructs called watchers can place a message on your screen (center) to warn you when a design change violates a project constraint.*

The Concurrent Design Environment, an umbrella term for all Mentor Graphics' and compatible third-party CAD and CAE products, automates product design to a degree never before possible. Key to this automation is the company's CAD framework package, dubbed Falcon. The Falcon framework for concurrent design forms the core of the company's latest product introductions, known collectively as Software Release 8.0. Falcon helps engineering organizations plan and coordinate product development in the following ways: It provides a consistent user interface for all design tools; it stores all project-related information in a unified database; it provides project-team members with ready and controlled access to that data; and it automatically monitors all design activity to ensure fulfillment of project goals.

The Falcon framework comprises four components: an extended version of the Open System Foundation's Motif graphical user interface (GUI) for Unix, a design data-management system (a database manager), a design-management environment, and a decision-support system. The common user interface and unified database provide a foundation for all of Falcon's tools.

By incorporating Motif, Falcon provides a standard method for CAD and CAE tools to interact with a designer through windows and menus. However, GUIs can hinder an advanced user's ability to perform at maximum efficiency by throwing a seemingly endless series of menus in the way. Mentor added several extensions to Falcon's GUI such as a pop-up command line, prompt bars, a user programming language, and hypertext-based help screens to address this potential problem.

Falcon's GUI unifies EDA (electronic design automation) tools at the topmost level; Falcon's database provides consolidation at the lowest level. The database manager stores all design data in object-oriented data structures. These structures respond identically to requests by design tools, design-management programs, and user commands. More important, however, the unified database eliminates data-format incompatibility among Falcon-compatible CAD and CAE tools.

Falcon's design-management environment provides engineering managers with version-control, configuration, and product-release facilities. Using this tool, engineering managers can ensure that all project engineers use the correct versions of the appropriate tools (as determined by the project team). You can also control product releases to ensure that the proper versions of all the right parts—and none of the wrong ones—get into each product release. Software products from other companies have provided such control, but it's an integral part of the Falcon framework.

The decision-support system is a universal modeler with many fundamental uses. An integral spreadsheet provides the computational power for the decision-support system. The spreadsheet can automatically calculate factors such as cost or power dissipation for your product. It can even perform thermal analysis. The decision-support system automatically extracts the data needed to solve the spreadsheet equations from Falcon's unified database. For example, the project's bill of materials and a component database supply the spreadsheet with enough information to simultaneously compute a product's MTBF, power dissipation, and cost.

However, the decision-support system does far more than the spreadsheet paradigm might imply. Using pictorial elements such as meters and numeric displays, the decision-support system can paint a real-time appraisal of the spreadsheet's results on your screen. You might, for example, tie the image of a VU meter to your project's cost as computed by the spreadsheet. You can then incorporate your cost goals into that representation by defining a red zone on the meter to represent excessive cost. Thus, when you look at the meter, you can see whether or not your project is exceeding its cost limits and meeting its goals.

Similarly, you can hook your product's computed MTBF, power dissipation, size, radiation budget, or any other quantifiable metric to a meter or another type of display. In effect, the decision-support system allows you to create a control panel that helps you manage your whole project.

The same system, through a mechanism called a watcher, allows you to define situations that pop up a warning message on any designated team member's screen if a design change violates a project constraint. This type of information helps your project team make informed decisions regarding component selection, hardware/software tradeoffs, standard-vs-optional feature selection, and related product-development decisions that previously were made with a more seat-of-the-pants approach.

The decision-support system also allows you to model your entire product through the spreadsheet and paint a working, simulated front panel on your screen complete with live displays and working controls. (You activate the controls by pointing to them and clicking them on with your workstation's mouse.) You can define a "living" product specification with this system in a few days. Because everyone on the team can then see how the product is supposed to work, you should be able to slash the time needed to refine the product's definition and reach a consensus. The simulated product should also reduce the definition problems and ambiguity that plague paper specifications and cause projects to slip past deadlines.

The company is making the Falcon framework an integral part of its EDA tools. For example, Mentor's Board Station 8.0 Software Release includes Falcon along with other features such as an editor that adds automatic routing to the manual pc-board trace editor. The editor allows you to sketch a rough path to show the router where to place a trace. The editor's router will then squeeze through available paths and shove existing traces aside when necessary while concurrently performing design-rule checks.

The Board Station 8.0 Software Release will be available in the third quarter of 1990. Its price starts at $82,900 and includes an entry-level workstation with 16M bytes of RAM. Other members of the Software Release 8.0 tool family include products for IC design, cable layout, packaging design, software development, document creation and distribution, and thermal analysis. Prices for these tools will be announced in the second quarter of 1990.—***Steven H Leibson***

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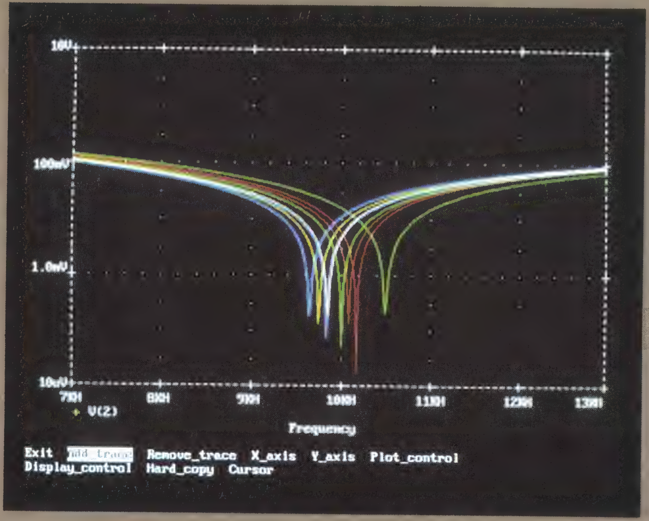

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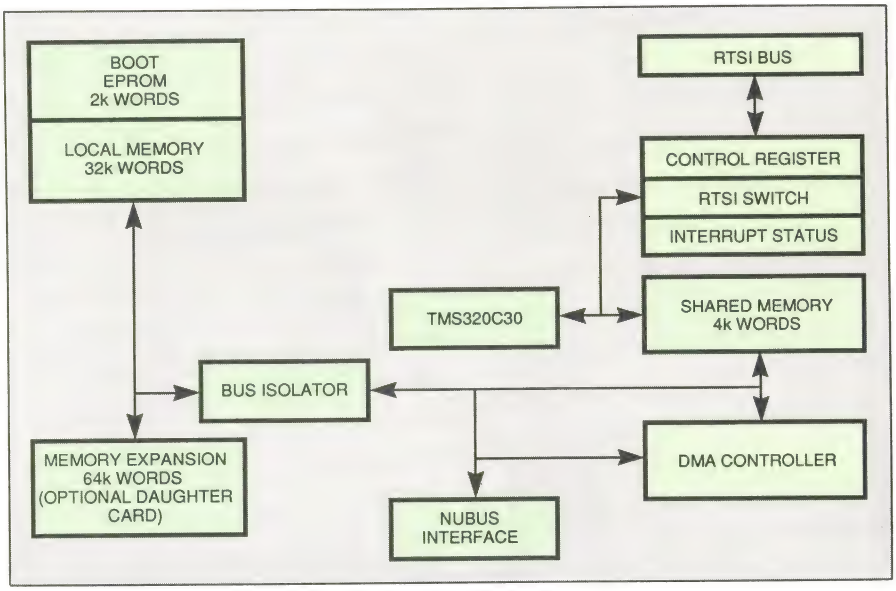
DSP board for Mac II yields 33M flops

If you've been looking for a dedicated, high-speed computation engine for your Macintosh II computer, try plugging in an NB-DSP2300. At the heart of this board is a 33.33-MHz TMS320C30 DSP μP, which has specs reaching 33M flops and 16 MIPS with 32-bit floating-point and integer precision. Incorporating an on-chip DMA controller, the TMS320C30 offers 60-nsec, single-cycle instruction execution and uses a 4-stage instruction pipeline that transparently manages processing conflicts. In addition, the IC can directly access any Nubus address space via the board's Nubus Master interface.

The board's DMA controller performs block-mode transfers as fast as 33.7M bytes/sec between the local memory and your Mac's Nubus. The $4995 board comes with 32k × 32-bit words of zero-wait-state static RAM that both the TMS320C30 and the Nubus can access. Furthermore, the board's 4k words of no-wait-state, dual-ported memory permit simultaneous access to the Nubus and the TMS320C30. For $5795, the board comes with 64k words of memory.

The DSP board uses a Real-Time System Integration (RTSI, pronounced rit-see) bus for interboard communications, such as external DMA requests and external interrupt requests. The RTSI bus also contains timing lines for synchronizing multiple NB-DSP2300 boards. Because the TMS320C30 uses a proprietary floating-point format, the NB-DSP2300 provides hardware to translate the chip's floating-point numbers into the IEEE floating-point format used by your Mac II.

Applications for the NB-DSP2300 include real-time signal analysis, filtering, spectral analysis, complex process control, high-resolution graphics, and imaging. The board occupies one Nubus slot in your computer. For $895, you can purchase the C30 Analysis Library, a library of 32-bit, single-precision software routines for the board, such as waveform analysis and generation, Fourier and spectral analysis, digital-filtering functions, statistical analysis, vector and matrix algebra, numerical analysis, and array functions. This software package provides language interfaces for Think-C 4.0 and MPW-C 3.0; however, you can use the C30 Analysis Library with any language that supports calls from the system-toolbox-device manager. The package also has a virtual-instrument interface for use with the manufacturer's LabView 2 instrumentation software. If you want to create new applications for the NB-DSP2300 board, you can order a $2500 developer's kit from the vendor.



Based upon a 33.33-MHz TMS320C30 DSP chip and a DMA controller that allows 33.7M-byte/sec data transfers, *NB-DSP2300 lets you perform real-time filtering and spectral analysis with your Macintosh II computer.*

If your applications require precise audio-frequency A/D and D/A conversions, you may also want to consider the $1595 NB-A2100 expansion board for the Mac II. It contains two 16-bit simultaneously sampling A/D converters, two 16-bit D/A converters, and a 16-word 32-bit FIFO buffer. The board's capabilities include antialias linear-phase filtering and sampling rates of 22.05, 24, 32, 44.1, and 48 kHz; harmonic distortion is typically below −95 dB for full-scale sine input from 20 Hz to 20 kHz. You can use the NB-A2100 to digitize or synthesize any signals within a 22-kHz-max bandwidth.—***J D Mosley***

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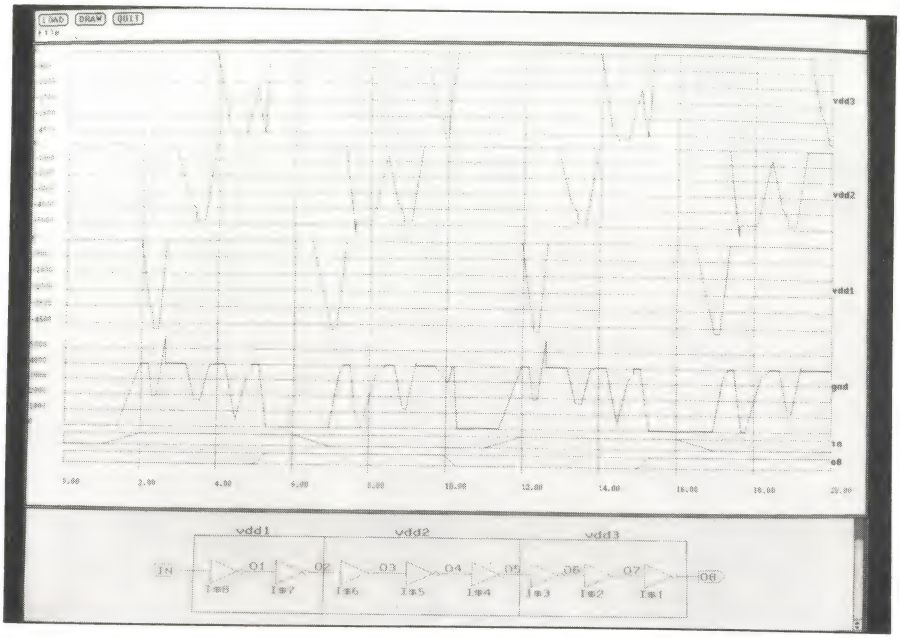
Circle No. 731

Power-analysis tool predicts digital chips' power consumption

The Powermill switch-level CAD tool analyzes node voltages, current flow, and power dissipation on your digital IC. Using this software, you can avoid haphazard analysis that leads to either overestimating or underestimating your design's current needs.

Overestimating your chip's current needs can lead you to add more power and ground pins than the chip needs. You might also build your supply rails too wide. Either of these actions can lead to more costly packaging decisions, including partitioning your design into more packages than is necessary. Conversely, underestimating current flow can degrade the performance and reliability of your IC.



When transistors switch on and off, *the instantaneous change in current flow can dramatically affect the supply rails, as this Powermill simulation output shows.*

Currently, two techniques are used to analyze power requirements. The most popular method estimates power consumption as the product of clock frequency, average device current, the number of transistors, and the probability of any one transistor switching. Another technique is to use Spice in one of its many variations. Spice is the simulator of choice for switch-level modeling of small- to midsized analog and digital circuit blocks. Unfortunately, as circuits get bigger, Spice gets overwhelmed, cutting throughput exponentially.

Powermill uses a first-order approximation of transistor characteristics to emulate power response. The tool calculates instantaneous and average current flow, power dissipation, and node voltages. Its models use more than 10 discrete voltage levels between logic 0 and 1 to drive its event queue.

Like a digital simulator, Powermill is event driven. However, a digital simulator's events are the single transitions between 0 and 1, whereas Powermill's events are the transitions between each discrete voltage level in the model. When an event occurs, the software uses the circuit's instantaneous node voltages to calculate the branch currents for all transistors. By summing currents, the software can compute total block and chip currents.

Powermill's analysis can guide the layout of your IC away from local high-current blocks. These blocks could lead to thermal problems and electromigration. Hot spots caused by high current flow can also affect timing and reliability. Electromigration, resulting from high-density electrons pushing metal atoms from the conducting trace into the insulating silicon dioxide, increases resistance and degrades performance and reliability.

You should also provide effective power distribution; otherwise many transistors switching simultaneously can cause a surge that temporarily depresses voltages with respect to ground. This surge can lead to device failure from effects like shrinking noise margins and ground bounce. To uncover these problems, Powermill uses short simulation patterns.

The software needs 8M bytes of RAM and runs on most popular Unix workstations. Powermill accepts files in Spice and Spice-like net lists. It has its own menu interface and waveform viewing package and is also encapsulated within both the Cadence Design Framework and the Viewlogic Workview framework. The power-analysis software starts at $35,000 for a single-user license.—***Michael C Markowitz***

Epic Design Technology Inc, 2900 Lakeside Dr, Suite 205, Santa Clara, CA 95050. Phone (408) 988-2944. FAX (408) 988-8324.

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IBM VGA graphics controller drives flat-panel displays

The Display Master VGA graphics controller can drive any of the four primary display technologies used with IBM-compatible personal computers. The card works with standard monochrome and color CRTs, and with EL (electroluminescent), ac plasma, and LCD flat-panel displays. Offering compatibility with IBM CGA, EGA, VGA, MDA, and Hercules graphics standards, the card supports maximum resolutions of 640×480 or 720×400 pixels.

Medical, industrial-control, test-equipment, and other applications commonly require flat-panel displays. Furthermore, designers are using personal-computer architectures more and more to get products for such applications to market quickly. The Yamaha V6388 controller chip forms the basis of the graphics controller card. Based on volume and time-to-market requirements, OEMs can choose between designing a graphics card with the chip or using the turnkey Display Master VGA card.

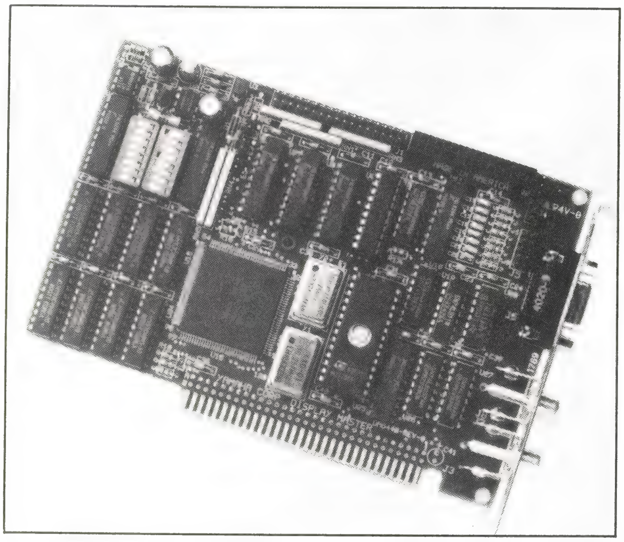
In addition to handling the normal 1-, 4-, and 8-bit displays, the Display Master VGA provides the 12 bits of color and integrated power supply to drive LCDs. An autoinitialization feature ensures that the card is set up properly before power is applied to a display.

The graphics controller supports alphanumeric and full graphics modes of operations. The card can map display frames that require less resolution to utilize all or part of a 640×480 screen. Furthermore, the card automatically converts color information to gray scale on monochrome LCDs, and to hatching on EL, ac plasma, and monochrome CRT displays.

An extensive manual included with the Display Master VGA details specific card settings you can use with more than 50 popular flat-panel displays. DIP switch settings allow you to customize the controller card for display type. The graphics card costs $395. Delivery, 60 days ARO.—***Maury Wright***

Yamaha Corp of America, 981 Ridder Park Dr, San Jose, CA 95131. Phone (408) 437-3133. FAX (408) 437-8791.

Circle No. 733



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Modem chip sets

Maury Wright, ***Regional Editor***

Like all application-specific ICs, new modem chip sets have higher levels of integration and lower prices than last year's models. Evolving modem chips also implement features defined by the CCITT (International Telegraph and Telephone Consultative Committee) standards committees that considerably raise the state of the art for modems. Standard error-correction and data-compression techniques reliably increase data throughput by 200%, 400%, and more. New modulation and encoding schemes make high-speed communications possible over lower-quality dial-up telephone lines. Available chip sets have begun to integrate data and fax functions, and the standards committees have started to bridge the two functions as well.

Advances in modem chip sets promise to make data- and fax-modem communications over the dial-up telephone network faster and more reliable. The chip sets now offer error-correction schemes and data-compression algorithms, and they use DSP to implement improvements in modulation and coding techniques.

Modulation and data-encoding schemes determine the raw throughput a modem offers. The **box**, "Data and fax communications depend on standards," summarizes the CCITT V.XX standards that define modulation and data-encoding schemes for data and fax modems. V.22 bis and V.32 define key international standards for full-duplex data communications at 2400 and 9600 bps, respectively. V.27 ter and V.29 specify half-duplex communications used in fax machines at 4800 and 9600 bps, respectively.

Modems feature DSP analog mix

Chip manufacturers implement the basic modem function, including modulator/demodulator and encoder/decoder, with a combination of analog circuits and DSP. Older modem chips, which communicate at less than 2400 bps, typically employ switched-capacitor-filter circuits to implement virtually all of the modem function. Available 2400-bps chip sets range from implementations with a heavy emphasis on analog circuits to ones that use DSP for everything but a couple of filters, an A/D converter, and a D/A converter. Modem chip sets that operate faster than 2400 bps all rely heavily on DSP.

Dwight Decker, Rockwell Semiconductor Products' director of data-modem products, points out that semiconductor manufacturers can shrink the digital circuits more easily than the analog ones. Therefore, the digital approach leads to faster transitions to higher levels of integration and lower cost. DSP-based µPs also benefit from advancements in general-purpose processors and therefore become faster and smaller, require lower power, and cost less—seemingly everyday.

Modem chip sets must also carry the baggage of prior-generation products. V.22 bis 2400-bps products, by market demand, include backward compatibility with 1200- and even 300-bps standards. Before achieving widespread acceptance, 9600-bps data modems will include fall-back capabilities all the way to 300 bps. Such backward compatibility ensures that a modem can connect with virtually any other modem, despite differences in modem capabilities and line conditions.

Modem designs that use a simple general-purpose AFE (analog front end) and rely heavily on DSP essentially implement the modem function in software. Therefore, support for older standards requires nothing more than memory space in the modem design once the appropriate DSP algorithms are developed.

New modem chip sets use DSP to integrate data- and fax-modem functions. (Photo courtesy Exar Corp)

Manufacturers of modem chip sets have used mixtures of analog circuits and DSP for low-speed modems, but modems faster than 2400 bps rely heavily on DSP.

Analog approaches require different analog circuits for each different standard that a modem supports.

Despite the promise DSP offers, don't choose a modem chip set simply because of labels for modem architecture. Rather, choose a chip set based on your needs and such criteria as raw performance (the ability of a modem chip set to perform at full specified speed over noisy lines), level of integration (the chip count required to implement a specific modem function), degree of flexibility (the degree to which you can add functions, and therefore value, to your modem design), price, compatibility (hardware and software compatibility with target applications such as personal computers and the industry-standard Hayes command set), time-to-market requirements, power requirements, error-correction capability, data-compression features, and integration of data and fax modem capabilities.

You have to judge the raw performance needed for your application. Unfortunately, you won't find comparable specs from all the manufacturers that indicate how well a chip set performs over noisy lines. In general, however, modem performance has improved with new modulation schemes, despite increasing bit rates and a fixed-signal bandwidth.

Chip sets offer integration tradeoffs

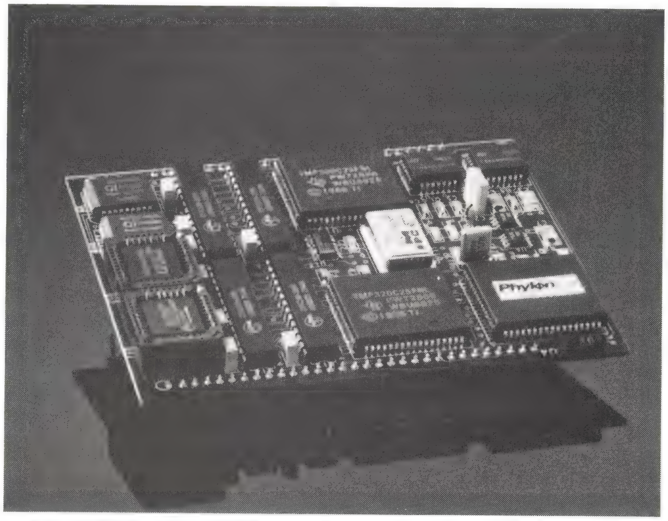
Typically, you must make tradeoffs when considering level of integration, degree of flexibility, price, and compatibility. For example, Sierra Semiconductor Corp offers several 2-chip sets that implement a complete Hayes-compatible 2400-bps modem. The AFE chip includes the modulation capabilities. A controller chip implements adaptive equalization using DSP and includes the Hayes-command-set firmware. The SK0620 chip set costs as little as $51 (100), and you only need to add a DAA (data-access arrangement), which isolates the modem and phone line, to complete the modem. The chip set includes the UART required for Hayes compatibility and the 2- to 4-wire converter that interfaces with the DAA.

Silicon Systems Inc takes a different approach. It targets flexibility with its designs. For example, the SSI 73K224 IC includes an AFE and a custom μP core with DSP routines in firmware. The IC costs $23.50 (10,000), but you also need a microcontroller, the microcontroller software, a UART, and the DAA to fully implement the modem. The company supplies software, in source-code format, that allows you to implement a Hayes-compatible modem with Intel microcontrollers. If you need to add features to a modem's capability, you may find working with industry-standard Intel microcontrollers preferable to Sierra's proprietary controllers.

Time-to-market requirements may make modem chip sets an inappropriate route to follow completely. Companies such as Cermetek, Xecom, and Rohm offer off-the-shelf modules that include complete modem implementations. Modules provide the advantage of complete FCC approval. Also, claims Cermetek CEO Howard Raphael, modules make economic sense at volumes under 5000 units. Cermetek will provide custom modules in volumes as low as 500 units.

Modem IC manufacturers have made significant improvements in their chips' power requirements, making them more suitable for portable and battery-powered applications. Sierra now offers virtually all of its chip sets in 5V-only versions. Intel's new 89C024 V.22 bis 2-chip set includes two power-down modes. The 5V-only chip draws 400 mW. The chip set employs Intel's 83C196 microcontroller, which has a standby mode, to reduce power consumption to 255 mW. The microcontroller also has an idle mode, which shuts down the clock to the AFE chip and reduces power consumption to 1 mW. The chip set costs $32 (1000) and requires a 256k-byte ROM in addition to a DAA to complete the modem function.

Error correction and data compression are the most



The dual 320C25-base PHY-96 module from Phylon offers compatibility with data- and fax-modem standards at speeds as fast as 14,400 bps.

exciting new developments for modems. Error correction implemented in modem chips eliminates overhead in throughput caused by error checking at the application-software level and eliminates retransmission of bad data. Data compression simply doubles or quadruples the effective bit rate that a modem offers.

MNP offers error correction and compression

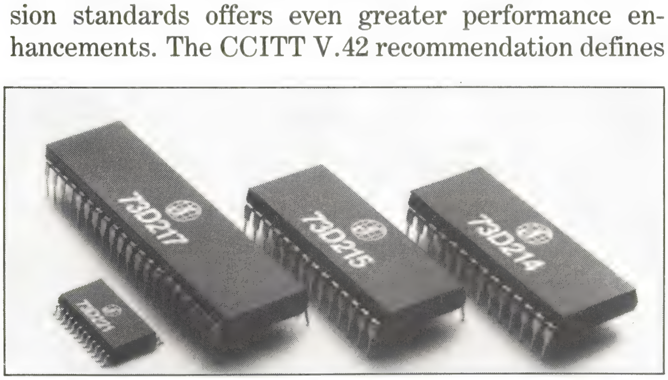
Currently, manufacturers offer modem chip sets that comply with de facto standard MNP (Microcom Networking Protocols) levels 2 to 4 for error correction and level 5 for a 2:1 data compression. Intel's 89C024, for example, implements these protocols. The data-compression feature requires the addition of an 8k-byte static-RAM buffer to perform the compression operation. Sierra adds MNP 2 to 5 capabilities to its chip sets by adding an additional processor, ROM, and RAM. Sierra plans to ship a chip set later this year with a single controller that handles normal modem and MNP functions.

Exar Corp offers its $18.51 (10,000) V.22 bis modem that includes a DSP μP (a mask-programmed TI TMS 320C10) and an AFE. An Intel microcontroller completes the typical modem. MNP applications, however, require the use of the XR-2403 microcontroller, which raises the price to $25.97 (10,000). Also, you must add ROM and RAM to complete the MNP functions. You do receive added flexibility with the Exar chip set, however. Sophisticated OEMs could add customized code to the commercial DSP μP used in the chip set to add, for example, compatibility with new encoding schemes.

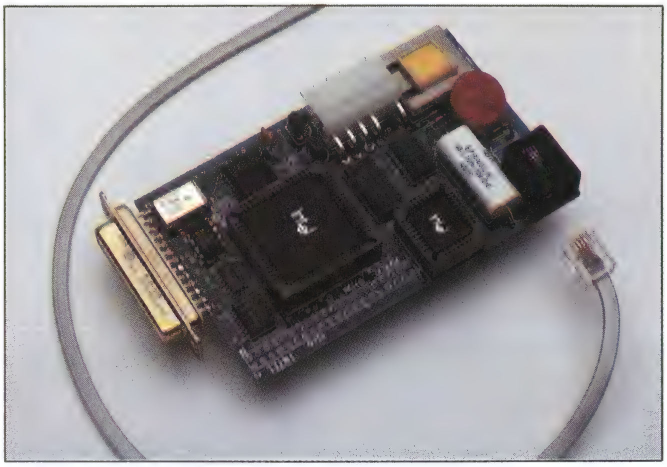
You can see that MNP adds another factor to the integration, price, and compatibility tradeoffs. Though MNP capabilities have been around for several years, they're just now gaining widespread acceptance. Unquestionably, they more than double effective modem bit rates.

A second set of error-correction and data-compression standards offers even greater performance enhancements. The CCITT V.42 recommendation defines an error-correction scheme that includes both MNP 2 to 4 capabilities and the capabilities included in LAPM (link-access procedures for modems) adapted from IBM SDLC (synchronous data link control). Furthermore, V.42 bis defines a new data-compression scheme that offers a 4:1 compression ratio. A 2400-bps modem essentially operates at 9600 baud when equipped with V.42 bis. Likewise, a 9600-bps V.32 modem attains effective speeds of 38,400 bps.

Technology licensing issues may slightly cloud the future of V.42 bis, however. IBM, Unisys, and British Telecom all hold patents that relate to V.42 bis technology. CCITT requires that a company promise to license technology in a "fair and nondiscriminatory" manner before it adopts proprietary technology into a standard. Currently, the three companies plan to charge $15,000 to $20,000 each for licenses. Modem-chip manufacturers would prefer to negotiate licenses that include a "pass through" to their customers. The customers would prefer pass-through licensing as well. Unfortunately, the present proposal requires each manufacturer of V.42 bis products, such as a modem board for a personal computer, to buy a license. By the time this article appears, industry sources say, these issues should be resolved.



The MNP 2 to 5 compatibility in Silicon Systems' 73D2407 chip set can more than double the effective throughput of the 2400-bps modem.



The Intel 89C024LT chip set, with its idle-mode capability and 1-mW power consumption, is ideal for battery-powered portable applications such as laptop computers.

Chip set includes V.42 and V.42 bis

Legislative issues aside, modem-chip manufacturers have proceeded to develop V.42 and V.42 bis chips, with Rockwell being the first manufacturer to announce such a chip set. The RC2324AC includes MNP 4 and V.42 error correction and MNP 5 and V.42 bis data compression. The V.22 bis 2-chip set maintains

Text continued on page 100

Data and fax communications depend on standards

More than any other segment of the computer and electronics industry, communications capabilities depend upon—in fact don't work without—standards. Below are some key standards for data and fax modems, along with information on the standards organizations. Beware, however. This list may very well be added to or otherwise changed by the time you read this article.

Primarily, two organizations administer data- and fax-modem standards. Formerly part of the Electronic Industries Association, the TIA (Washington, DC (202) 457-4936) now handles modem and other communications standards in the USA. The CCITT administers modem and fax standards in Europe, and increasingly is being recognized as a worldwide bearer of communications standards. It is part of the International Telecommunications Union (Geneva, Switzerland (Phone 41 22 995111).

Fortunately, TIA committees TR-29 (fax) and TR-30 (data) in the USA work closely with CCITT study groups abroad. The TIA committees essentially funnel the desires and opinions of organizations in the US to the CCITT study groups. Furthermore, some organizations in the US send delegates to CCITT meetings. And the TIA endorses and adopts appropriate CCITT recommendations (the CCITT term for standards) for use domestically.

The CCITT publishes recommendations in a series of books once every four years. Each set of books has different colored binders. The set published in 1988 is blue; white ones will follow in 1992. Once a year the CCITT study groups also meet and approve recommendations on an individual basis. "T"-series recommendations address "terminal equipment for telematic services," including fax. "V"-series recommendations address "data communication over the telephone network," including data modems.

Unfortunately, standards practices weren't always so uniform internationally. Accepted US standards for 300- and 1200-bps asynchronous data communications differ from CCITT recommendations. Furthermore, some published recommendations are used prevalently in some parts of the world but not in others.

Fax-transmission standards

T.4 (pronounced "T dot 4") specifies 200-dpi fax-transmission capabilities commonly referred to as Group 3. The T.4 document references V.27 ter and V.29 to define modem speed and modulation.

T.5 specifies Group 4 fax capabilities, which include support for 400-dpi resolution and alternate page formats. T.5 provides for several transmission media, including ISDN (Integrated Services Digital Network), the public-switched telephone network, packet-switched public-data networks, and circuit-switched public-data networks. T.5 adds substantial complexity to simple T.4 fax communications over dial-up lines. And, because of media incompatibilities among users, it may never become a mainstream technology.

T.30 ECM (error-control mode) defines an enhancement to Group 3 fax that provides a data-link-layer, error-control protocol.

V.14 specifies a method to perform character-asynchronous transmissions over synchronous interfaces. The V.XX standards for data modems reference V.14.

Low-speed modem standards

V.21 and **Bell 103** specify 300-bps 2-wire full-duplex communications using FSK (frequency-shift keying) modulation schemes. AT&T created the Bell 103 specification during the days of telephone-system monopoly in the USA. The standards differ slightly, but virtually all of today's modems support both standards. Asynchronous modems based on these standards dominate applications worldwide for 300-bps dial-up modems—such as personal-computer modems.

V.22 and **Bell 212A** specify 1200-bps 2-wire full-duplex communications using QPSK (quadrature-phase-shift keying) modulation schemes at 600 baud. The standards differ slightly, but virtually all of today's modems support both standards. Asynchronous modems based on these standards dominate applications worldwide for 1200-bps dial-up modems.

V.22 bis specifies 2400-bps 2-wire full-duplex communications using a QAM (quadrature amplitude modulation) scheme at 600 baud. Asynchronous modems based on these standards dominate applications worldwide for

2400-bps dial-up modems.

V.23 specifies an asymmetrical communication scheme that implements 1200-bps data transmission in one direction and 75-bps data transmission in a back channel. The FSK-based standard is popular in Europe for applications that require high data rates in only one direction, such as Teletext.

V.24 specifies a serial interface much like RS-232C.

V.25 and **V.25 bis** specify interface protocols for modems similar to the command set Hayes Microcomputer Products (Atlanta, GA) employs in its modems.

V.26, V.26 bis, and **V.26 ter** specify half- and full-duplex leased-line communications at 1200 and 2400 bps. The specs employ QPSK modulation at 1200 baud. V.26 ter was the first modem standard to specify echo cancellation.

High-speed modem standards

V.27, V.27 bis, and **V.27 ter** specify 4800-bps communications requiring two wires for half-duplex applications and four wires for full-duplex applications. The standards specify QAM modulation at 1600 baud. Group 3 fax standard T.4 references V.27 ter as the base requirement for 2-wire half-duplex fax communications.

V.29 specifies 9600-bps communication requiring two wires for half-duplex applications and four wires for full-duplex applications. The standard specifies QAM modulation at 2400 baud. Group 3 fax standard T.4 references V.29 as an option for fax transmissions faster than 4800-bps V.27 ter. In reality, a high percentage of fax transmissions today rely on V.29, although virtually all machines can fall back to V.27 ter.

V.32 specifies 2-wire full-duplex 9600-bps communications using QAM modulation at 2400 baud and echo cancellation. V.32-based modems offer an upgrade path from V.22 bis for asynchronous dial-up applications. Recently V.32 Automode was published as an annex to V.32. The annex defines an automatic fall-back capability to V.22 bis on noisy lines that can't support 9600-bps communications.

V.33 specifies 4-wire full-duplex and 2-wire half-duplex communications at 14,400 bps. Most likely, the Group 3 fax study group will modify T.4 this spring to include V.33 14,400-bps communications as an option. Likewise, you can expect manufacturers of full-duplex data modems to add echo cancellation and take advantage of this spec. V.33 employs TCM (trellis-coded modulation) at 2400 baud.

Communications enhancements

V.42 specifies error-correction techniques that can be implemented in modems independently of transmission speed and modulation scheme. The recommendation includes LAPM and MNP 2 to 4 (Microcom Networking Protocol) methods of error correction.

V.42 bis and MNP 5 specify data compression algorithms that can be implemented in modems independently of transmission speed and modulation scheme. MNP 5 has not been recognized by standards organizations but has become a de facto standard for data compression that offers a 2:1 compression ratio. V.42 bis offers a 4:1 compression ration and products that implement the standard are starting to emerge.

V.54 specifies loop back and other diagnostic functions for modems.

Several other potential developments bear mention also. Fax study groups have worked on a standard for binary file transfers using a fax modem. Several manufacturers of fax boards for personal computers now offer proprietary methods of transferring files at high speed. Expect formal approval of such a standard no later than next spring.

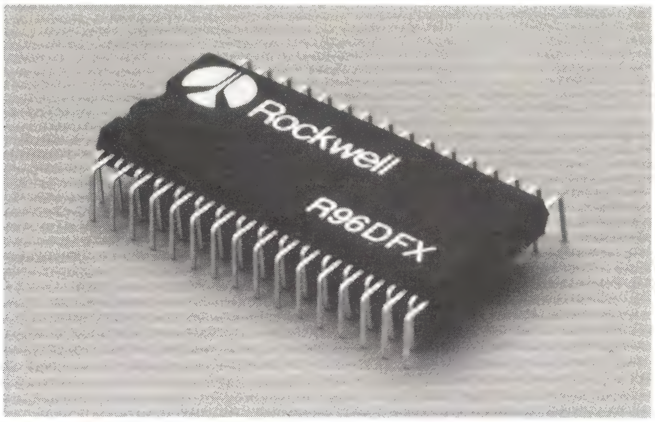
Likewise, study groups have discussed adding a provision for higher resolution to the T.4 fax standard. T.4 currently supports 200-dpi resolution, and you can expect 400-dpi capabilities to be added no later than next spring.

Unless you happen to be a member of a TIA committee or a delegate to CCITT study groups, you may have a hard time tracking communications standards. The *Communications Standards Review* newsletter (**Ref 1**), published by Action Consulting, covers all pertinent activity in domestic and international committees. You can also purchase copies of communications standards from Action Consulting (Palo Alto, CA (415) 856-8836).

downward compatibility with lower-speed standards and offers compatibility with the asymmetrical V.23 standard popular in Europe. Packaged in two 68-pin PLCCs (plastic leaded chip carriers), the chip set costs $35 (10,000). One of the chips integrates an AFE and DSP core. The other chip includes a microcontroller that implements the error correction and data compression. You must implement Hayes compatibility for the chip set in another microcontroller. Rockwell also plans to sell the DSP/AFE chip as a stand-alone data pump.

Achieving the lowest possible chip count for modem designs may necessitate tradeoffs in design flexibility and cost.

Silicon Systems has also developed, in conjunction with Hayes Microcomputer Products (Atlanta, GA), a modem chip set that supports V.42 and V.42 bis. Hayes has introduced a modem based on the chip set; Silicon Systems intends to sell the chips as well. Sierra, Exar, and Intel all plan to have V.42 bis chip sets available after midyear. In general, expect the new chip sets to use more powerful microcontrollers, more buffer RAM, and more ROM than their MNP 5 cousins.



Compatibility with T.30 ECM allows Rockwell's R96DFX Monofax chip to correct transmission errors and therefore produce higher-quality fax images.

Techniques such as MNP 5 and V.42 bis may slow the industry transition from 2400- to 9600-bps products. Currently, only Rockwell offers V.32 9600-bps chip sets for data communications. Still, prices to the end user for 9600-bps modems have dropped below $700, and the downward trend should continue. You can expect Sierra to introduce 9600-bps data modems in the first half of this year. In addition, Yamaha Corp may add data capabilities to its 9600-bps fax-modem chip.

Fax-modem-chip manufacturers Rockwell and Yamaha offer 9600-bps chips that comply with V.29 and V.27 ter. Furthermore, Toshiba and Hitachi recently introduced 9600-bps fax chips. Fax modems are inherently simpler than data modems because fax modems employ only half-duplex communications, whereas a 9600-bps data modem employs echo cancellation to perform full-duplex communication over a single signal band. Group-3 fax modems also have fewer old standards to maintain compatibility with than do data modems.

Rockwell's newest 9600-bps fax chip, the R96DFX Monofax, requires no external components to support HDLC (high-level data-link control) framing and DTMF. The device costs $48.50 (10,000) and is packaged in a 64-pin quad-in-line package. The chip also supports the new ECM (error-correction method) defined in T.30 for fax communications. The R96DFX can directly replace earlier Monofax chips.

Rockwell long had the fax-modem-chip business to itself. Now, however, Yamaha is gaining in market share since introducing its YM7109 9600-bps fax modem chip. The IC includes both a DSP core and an AFE; it sells for $38 (10,000). The chip operates from a 5V supply and only consumes 180 mW of power.

Yamaha has had particular success selling the YM7109 into the fax-board market. An OEM can manufacture a nonintelligent fax board for the IBM PC for less than $60. Some Yamaha customers sell such fax boards to end users for less than $200. Later this year, expect more fax-modem chips from Yamaha that include features such as power-down modes, T.30 ECM support, and more integrated features for fax-machine applications such as a scanner interface.

Fax modem offers 14,400-bps transfers

Rockwell, meanwhile, has upped the ante with a chip set that supports fax communications at 14,400 bps. The 5-device set complies with V.33, and you can expect the T.4 Group-3 fax spec to add V.33 as an option this year. Expect prices for the chip set in the $200 (10,000) range.

Fast and reasonably priced fax-modem chips have spurred interest among users that need faster data-communication speeds. Study groups in the TIA (Telecommunications Industry Association) and CCITT are considering adding a protocol for binary file transfers to fax standards. The half-duplex fax communication scheme could be turned around using a "fast train" capability and offer pseudo full-duplex communications. Another option might use a 300-bps back channel to establish asymmetrical communications.

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V.42 bis promises to boost data rates by a factor of four, but licensing issues may delay widespread acceptance of the data-compression standard.

The line between fax and data modems is growing increasingly thin. Several companies offer or soon plan to offer chip sets that implement data and fax communications. Rockwell currently offers a bundle of data and fax chip sets integrated together. Sierra offers a data-modem chip set with 4800-bps fax-send capabilities. Sierra will up the fax-send capability to 9600 bps and later this year will add full send/receive capability.

Exar wins the race to introduce a highly integrated combination fax- and data-modem chip set. Its XR-2900 2-chip set includes a 40-pin DSP-based chip and a 48-pin combination analog/digital chip that includes A/D, D/A, and filter functions. The chip set costs $27.33 (10,000) and requires a separate microcontroller for stand-alone operation. The chip set offers compatibility with V.22 bis and slower data communications. It includes support for V.29 and V.27 ter fax communications. Other features include a DTMF generator, remote and local test facilities, and automatic adaptive equalization. Exar plans to offer MNP 2 to 5, V.42, and V.42 bis support for the chip set. The company can also support capabilities such as binary file transfers at 9600 bps using proprietary protocols now and standard protocols when defined by CCITT.

One company, Phylon Communications, has gone one step further in terms of function—if not in terms of

Glossary of modem terminology

Adaptive equalization—A technique modems use to adjust for phase shift caused by the characteristic impedance of phone lines.

Asynchronous transmission—A method of transmitting data that allows a varying interval between transmission of characters—character asynchronous but bit synchronous. Start bits and stop bits indicate the beginning and end of each character. Also called start stop.

Bis—A term of Latin derivation that loosely means second.

Bit rate (bps)—The number of bits transmitted per second.

Baud rate—The number of discrete conditions or signal events per second.

Echo cancellation—A technique that allows full-duplex communications between two modems over the same signal band. A sending modem must cancel echoes from its own signal to decode a signal received from the other modem. The development of echo cancellation eliminates the need to split the overall signal bandwidth of a telephone line into send and receive bands.

Frequency-shift keying (FSK)—An FM technique that employs different frequencies to represent a binary 0 and a binary 1. FSK modulation results in one bit transmitted per baud.

Phase modulation—One of three basic ways (along with AM and FM) to add information to a carrier signal.

Phase-shift keying (PSK)—A phase modulation technique that employs discrete changes in phase to represent transitions from binary 0 to 1 or vice versa.

Quadrature PSK (QPSK)—A phase modulation technique that encodes two successive bits in a dibit. Each possible value of the dibit relates to a unique carrier phase shift.

Quadrature amplitude modulation (QAM)—A combination of phase and amplitude modulation that increases the number of encoded bits transmitted in a baud. For example, 16 discrete combinations of amplitude and phase encode 4-bits in a single baud.

Synchronous transmission—A method of data transmission that requires characters and bits to be synchronized.

Ter—A term of Latin derivation that loosely means third.

Trellis-coded modulation (TCM)—A modulation scheme that, like QAM, employs discrete combinations of amplitude and phase to encode data. But trellis coding uses data from three 7-bit bauds to encode six bits of data. Each baud contains coded information about itself, and about preceding and succeeding bauds. Math techniques similar to those used in ECCs for disk drives recover the coded data. The decoding process often used is called Viterbi decoding. TCM provides a 3-dB improvement compared with QAM.

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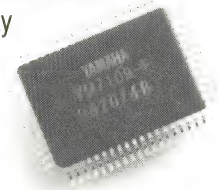
The YM7109 opens up a new world of applications. A FAX machine can answer phone calls and record messages. A PC can provide added utility as a FAX and telephone answering machine. Or a FAX board can greet callers and send requested information. The possibilities are endless.



But remember, those who get to market first — are the winners. That's where Yamaha's FAXSIM software gives you a head start.

It includes all the FAX modules, plus Bulletin Board Service using EIA Binary File Transfer/Bell 103, and ADPCM for storing and playing back voice. The source code is available in Turbo C™ and makes integration a breeze. Letting you move from design to production fast.

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integration level. Its PHY-96 Programmable Data Communications Module provides a glimpse into the future of communication chips. The module includes two TI 320C25 DSP µPs, a general-purpose AFE, ROMs, and other circuitry. The module measures 82×100 mm and offers plug-in compatibility with 9600-bps modules offered by Rockwell.

Modems have become software products that execute on DSP µPs with fairly generic analog components.

Phylon offers compatibility with all CCITT fax and data standards ranging from 300 to 14,400 bps. The module implements trellis coding at the 14,400-bps speed. The module costs approximately $200 (5000). The company builds a proprietary AFE, but is truly a DSP software company. Faster processors with denser memories eventually will replace dedicated application-specific ICs. And software companies will sell the key pieces to implement functions such as modems, voice synthesizers, and imaging systems.

References

1. *Communications Standards Review,* Action Consulting, Palo Alto, CA.

2. Bingham, John A. C., "The Theory and Practice of Modem Design," John Wiley & Sons, NY, NY, 1988.

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

Manufacturers of modem chip sets

For more information on modem chip sets such as those discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Hitachi America Ltd
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Brisbane, CA 94005
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Intel Corp
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International Microelectronic Products
2830 N 1st St
San Jose, CA 95134
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2001 Danfield Ct
Fort Collins, CO 80525
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Circle No. 665

Phylon Communications Inc
4027 Clipper Ct
Fremont, CA 94583
(415) 656-2606
FAX (415) 656-0902
Circle No. 666

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Newport Beach, CA 92658
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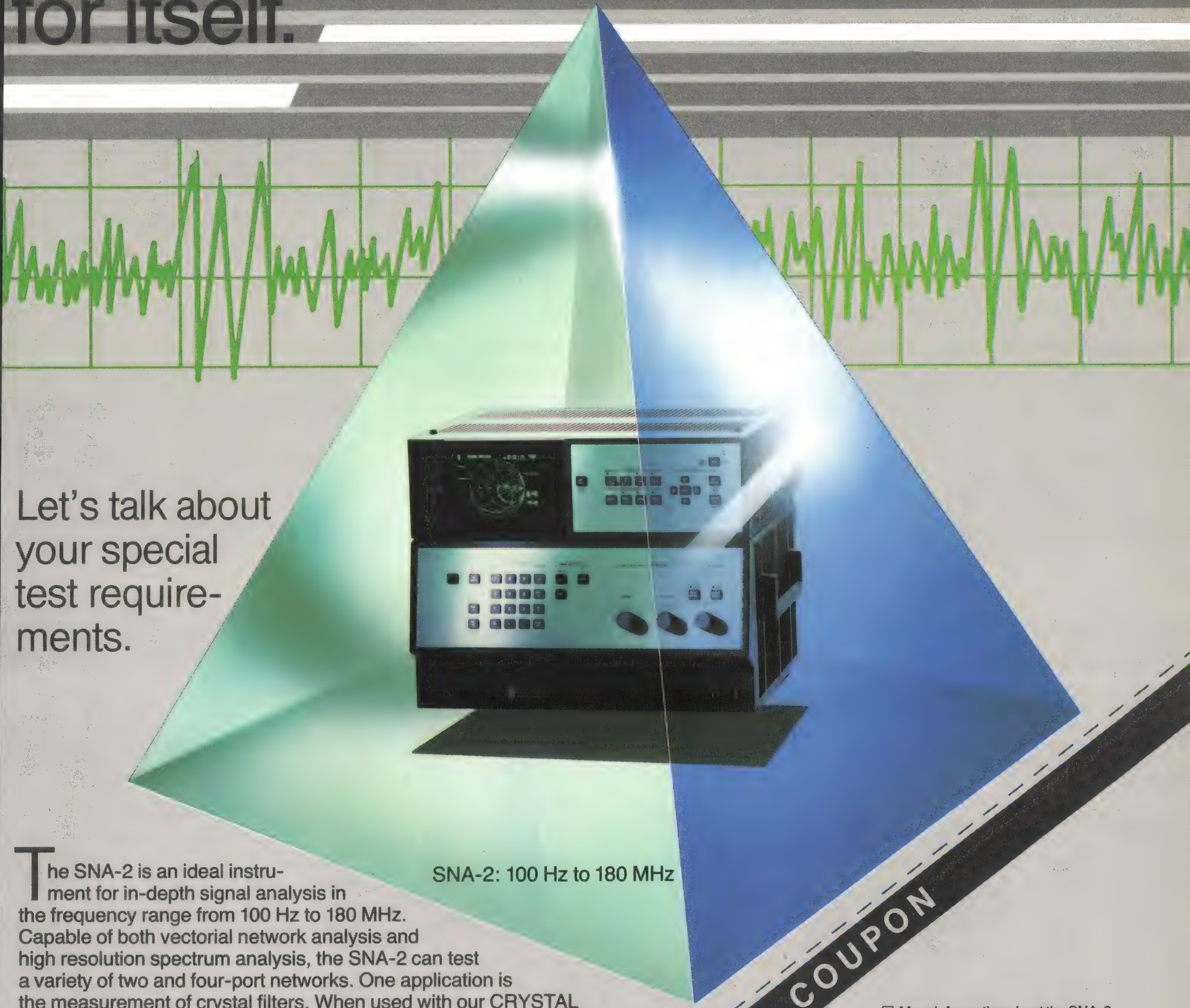

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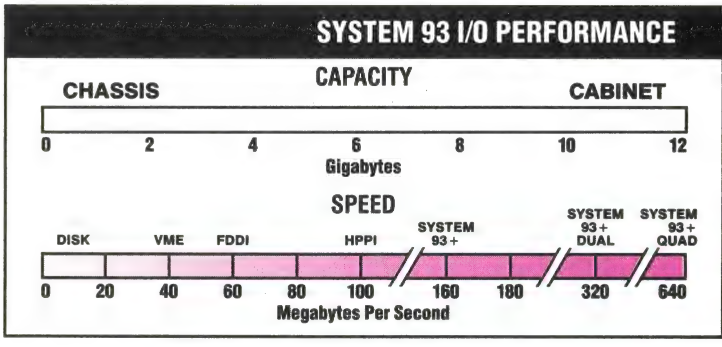

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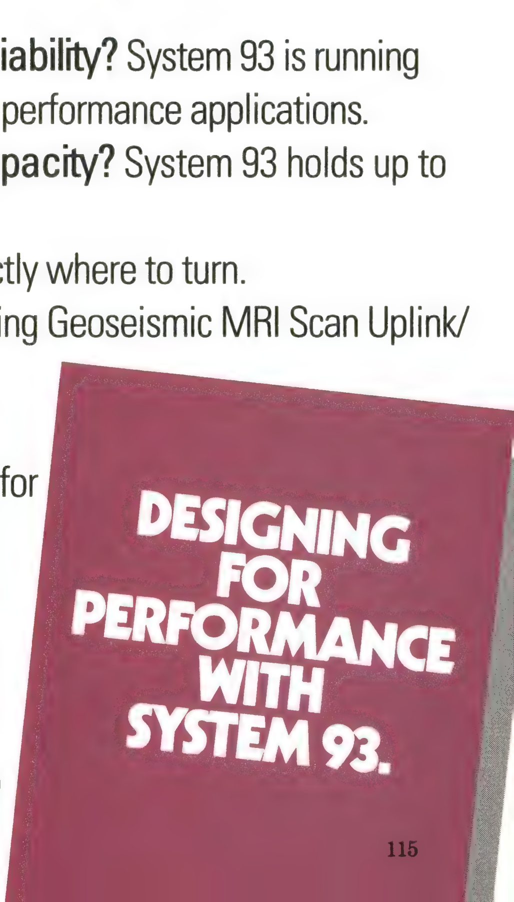

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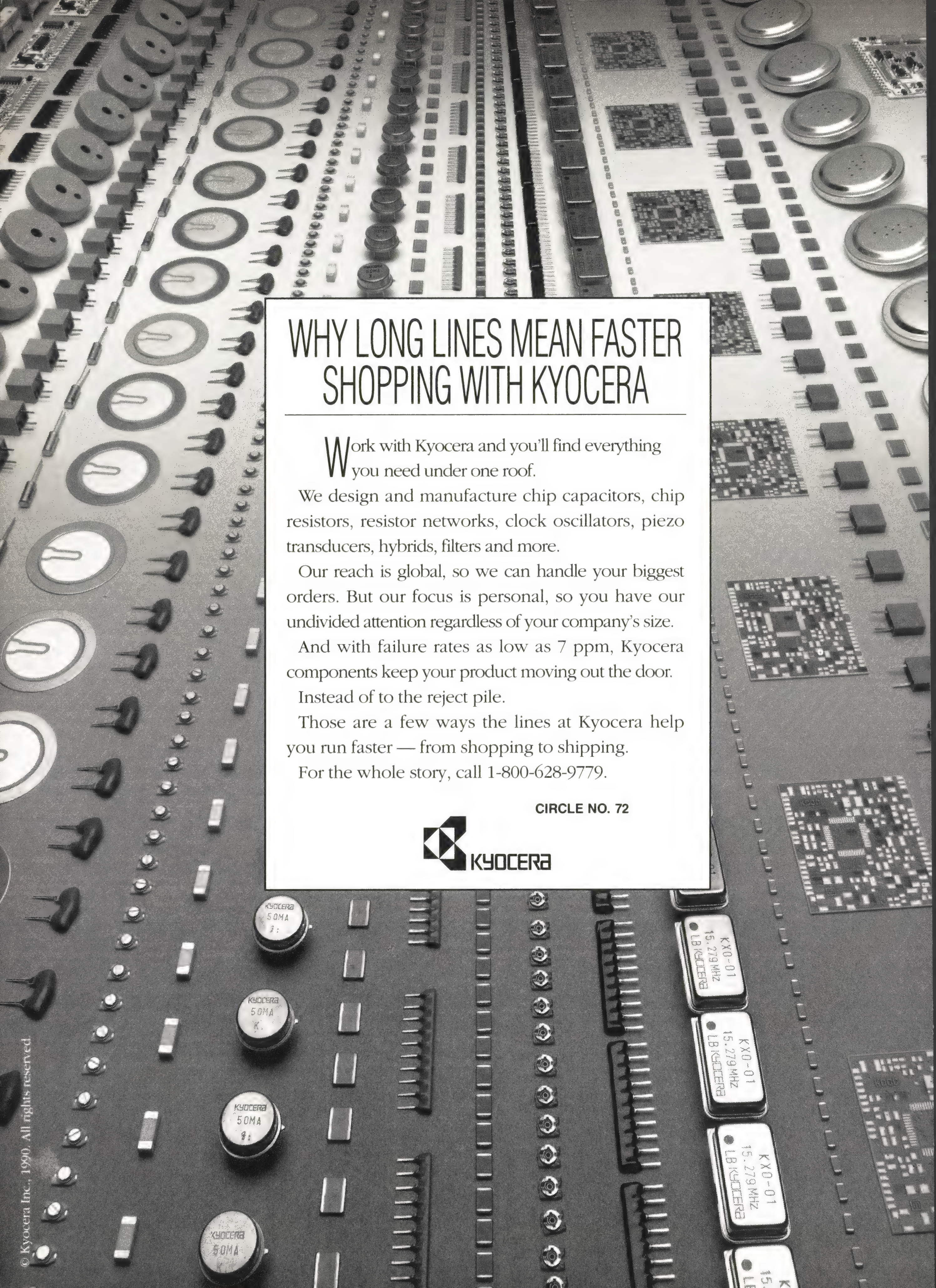

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EDN'S ALL-STAR PC

PART 3:

HUMAN INTERFACE

Nothing in computer design depends more on fuzzy factors, such as touch, feel, or shade, than the PC's human interface. Yet no ingredients affect the PC's utility more. A few standards exist for defining such human-interface factors as keyboard angle, key layout, and screen contrast, but these standards establish an ideal environment for that mythical person: the Typical User.

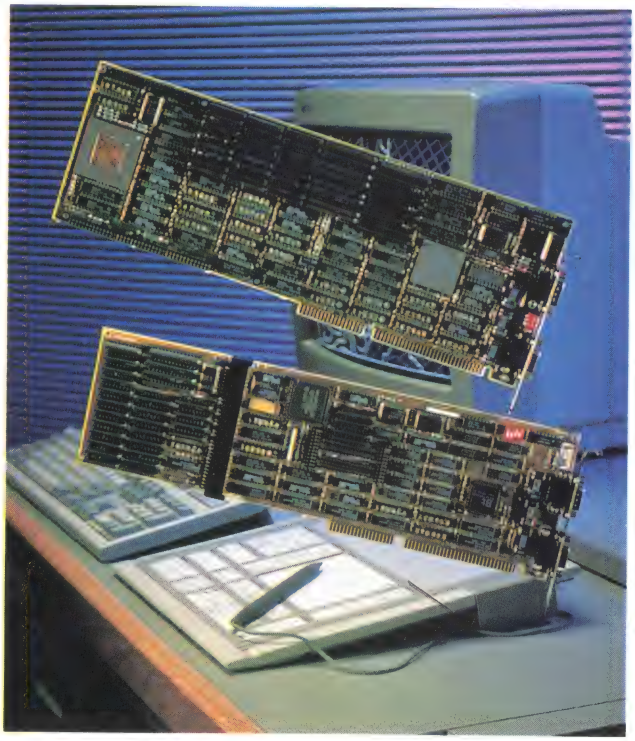
Designing the human interface is the toughest job in computer design. Every computer user has a valid opinion regarding the touch and placement of a keyboard's keys, the size and color of letters on the computer's display, and the feel of the linkage between the computer's mouse (or other graphics-input device) and the cursor on the screen. It is impossible for any one design to accommodate every user's preferences, so computer designers must compromise. PC-based workstations offer the best of all possible worlds regarding the user interface. A PC designer may standardize a computer's design around one keyboard, mouse, and display, but the PC's flexible architecture allows each user to change any of these elements for a more harmonious work environment. Because computers are supposed to enhance your ability to work, this flexibility is a key advantage for the PC-based workstation.

Selections made for the human-inter-

STEVEN H LEIBSON,
Senior Regional Editor

face components of EDN's All-Star PC reflect my own preferences. As a long-time microcomputer user whose experience predates the introduction of IBM's original PC, I've developed habits that the "average" or "standard" PC's user interface simply can't satisfy. Nowhere is the need for selection by personal preference more apparent than in the selection of the All-Star PC's keyboard, a Honeywell 101RX43S-12E. I evaluated several PC keyboards before selecting Honeywell's. Keyboard characteristics important to me include key placement and size, keystroke length, and tactile feedback.

Microcomputer users that started with RS-232C terminals expect to find the *Control* key next to the *A* key. Yet the standard PC/AT keyboard places the *Caps Lock* key in that location and consigns the *Control* key to the lower-left nether regions of the keyboard. Honeywell's keyboard is configured for the standard PC/AT placement, but the company also provides two key caps and a DIP switch on the back of the keyboard that allow you to switch the *Control* and *Caps Lock* keys (**Fig 1**). Individual users need that kind of flexibility. After all, there is no compelling reason why a computer cannot adapt to the user instead of the other way around.



Only a few components comprise a PC's human interface, but the keyboard, the mouse or digitizer, and the display card and monitor can make or break the computer's value. (Photo courtesy Hewlett-Packard Co)

The function keys are another example of keyboard-design elements that demand flexibility. IBM arranged the 10 function keys on the original PC keyboard in two columns running down the keyboard's left side. Many users, who first learned to use a computer by working with IBM's original PC, developed typing skills that included single-handed, 2- and 3-key chords combining the *Shift*, *Alt*, and/or *Control* keys with the 10 function keys. These users were disappointed when IBM moved the function keys on its PC/AT keyboard to a single row along the top, making those keyboard skills obsolete. Third-party keyboard vendors used that customer disappointment as an opportunity to sell add-on equipment and introduced PC/AT keyboards that retained the original double-column arrangement.

However, I prefer having the function keys across the top because I never developed those chording skills. My initial experience with function keys was on RS-232C terminals with the function keys across the top of the keyboard, like the "new" PC/AT arrangement. PC users can obtain keyboards that position the function keys either way.

Many different returns

Similarly, PC keyboards sport various types of return (*Enter*) keys. Some, like the original PC's, are unreasonably small; some look like an inverted letter "L" and resemble the return key on IBM's Selectric typewriters; and still others, among them the Honeywell 101RX43S-12E, have extra-large return keys for fumble-fingered typists like me. Other models in Honeywell's 101RX keyboard series have the inverted-L or small-size return keys, thus satisfying all preferences.

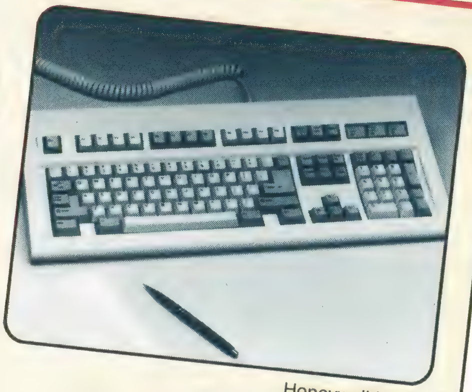
Obviously, PC users have a wide choice of keyboards, thanks to third-party manufacturers and the PC's de facto standard keyboard interface. Because the PC enjoys large sales volumes in the business market, you can pick from dozens of keyboard designs from several vendors with a range of key placements, sizes, and tactile feels. You can also find keyboards that incorporate graphics-positioning devices such as mice, trackballs, and finger digitizers. PC-based workstations do not force the user to type on the

EDN's PC All-Stars

101RX43S-12E Keyboard

Honeywell Keyboard Div, 4171
N Mesa Bldg D, El Paso, TX
79902. (915) 544-5511.

Circle No. 675



Honeywell Inc

STATS:

COMPATIBLE WITH: PC, PC/AT, PS/2

SWITCH TYPE: membrane

STATUS LEDs: num-, caps-, and scroll-lock

AUDIBLE FEEDBACK: electronic, switchable

FUNCTION KEYS: 12, arranged as one row

PEAK ACTUATION FORCE: 55g

BIO: The 101RX43S-12E features an enlarged return (**ENTER**) key, adjustable tilt, and switchable **CAPS-LOCK** and **CONTROL** keys, which allow an end user to tailor the keyboard for maximum comfort.

keyboard selected by the workstation's designer. Other computer workstations don't offer this advantage because their low sales volumes do not encourage keyboard-replacement offerings from third-party vendors.

EDN's All-Star PC doesn't use a keyboard with an integral-positioning device because that configuration would reduce some of the system's flexibility. By keeping the keyboard and positioning device separate, you allow your choice for each to be made independently of the other. Some users prefer mice, others like pen-and-pad digitizers, and some prefer trackballs. Even for one user, different applications may work better with different types of pointing devices. Mice make poor digitizers, but digitizers themselves may consume too much desk space for constant use. Even within a class of pointing devices, users have different preferences. Take mice, for example. Apple Computer would have you believe that all mice should have one button. Yet other companies sell 2- and 3-button mice, and at least one company sells a mouse with an entire keyboard built in. Which design is right? That depends on the application and the user. Once again, the choices available in the PC marketplace give you the most flexibility.

I prefer mice over trackballs and digitizing pads, so the All-Star PC uses a mouse for graphics input. PC mouse selection involves choices between mechanical, optomechanical, and optical versions with two, three, or more buttons. EDN's All-Star PC employs the optical PC Mouse II from Mouse Systems Corp. I like optical mice because of their feel and reliability. They have no moving parts and consequently don't fill up with dirt or lint and then stop working. Many people reject optical mice because they require a gridded mouse pad for operation and the pad consumes desk space. These same people often put a rubber mouse pad on their desk to improve traction for their mechanical mouse. Either way, mechanical or optical, the user—not the PC designer—can make the most suitable choice.

The PC's Darwinian displays

The range of choices that PC displays exhibit is also wide, but for evolutionary reasons rather than convenience. Since its introduction, the PC's standard graphics displays have evolved from the hopelessly crude CGA (color graphics adapter), which is suitable for playing low-resolution video games, to the VGA (video graphics array), which is adequate for design work. The standard VGA resolution of 640 × 480 pixels certainly supports acceptable CAE displays, and the extended VGA modes, which some vendors' cards now support, generate 800 × 600- or 1024 × 768-pixel displays and bring parity between PC and workstation screens.

However, all of the standard PC graphics cards including the VGA

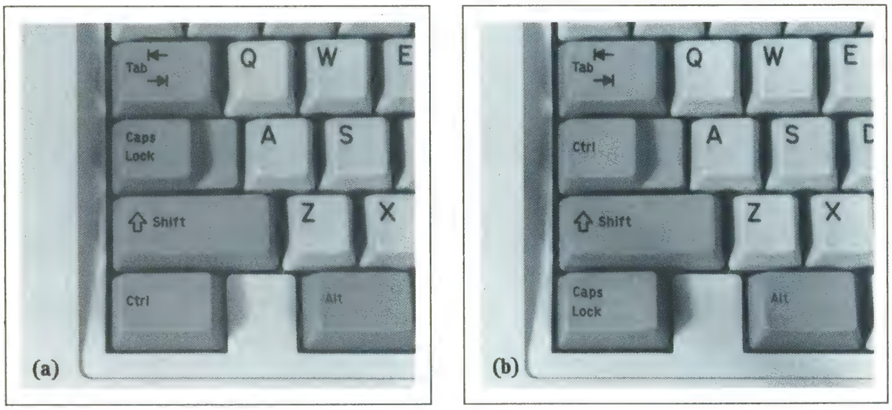


Fig 1—Conventional PC/AT keyboard layout places the caps-lock key next to the letter "A" key and banishes the control key to the lower-left corner of the keyboard (a). Honeywell's 101RX43S-12E PC-compatible keyboard allows you to exchange the positions of these two keys (b), making the keyboard less compatible but easier to use.

family suffer from a common failing: they're all dumb bit maps. The PC's CPU must paint every dot on the screen, one pixel at a time. Furthermore, the bit-map orientation of the PC's graphics-display cards has stymied the development of device-independent PC graphics. Two promising candidates to overcome these shortcomings are IBM's 8514/A and Texas Instruments' TIGA (Texas Instruments Graphic Architecture). Both of these designs employ display-list processing. An image to be displayed is stored as a list of graphics elements (such as lines, arcs, and polygons); the intelligent graphics card reads the display lists, clips the graphics elements to fit the screen, and then plots the resulting pixels on the display. Thus, an intelligent graphics card can perform zooms and pans without burdening the host CPU. For software written to take advantage of a graphics processor, the performance boost can be tremendous.

IBM's 8514/A graphics adapter card promises to become a de facto standard through the same mechanism that made the PC itself a standard: IBM's clout. Many companies have copied and improved upon PC products first introduced by IBM, but IBM didn't publish documentation for the 8514/A's hardware. In fact, it warned other companies that it might change the 8514/A's hardware design at some future time and asked software vendors to use the 8514/A's software interface, called the AI (adapter interface), to draw on the screen instead of writing directly to the 8514/A's hardware.

However, many PC-software vendors discovered that the 8514/A's AI was slow, so they bypassed the software interface and went straight to the display card's hardware. Accordingly, hardware vendors who wished to copy IBM's 8514/A display adapter reverse-engineered the board's hardware interface and settled on a common set of register-based specifications. These reverse-engineered specs freeze many elements of the 8514/A's design including the display's resolution and pixel depth, the interlaced scanning mode that IBM selected (which can produce flickering images), and most importantly, the display adapter's drawing commands.

Extensibility holds promise

IBM's 8514/A display adapter incorporates a μP, so it is an intelligent-graphics-display adapter. However, it is not programmable; its graphics routines are hard-coded into ROM, and its command set supports only one fixed resolution—1024×768 pixels. On the other hand, TIGA display boards based on Texas Instruments' 340 series of graphics μPs support many resolutions because TIGA's command set specifies resolution-independent graphics. TIGA also permits application-specific extensions to its command set for added performance. TIGA-based display cards keep their graphics code in RAM to support that extensibility. The TIGA-based display cards' range of flexibility makes them the right choice for the All-Star PC.

The All-Star PC incorporates three display cards: a VGA card to ensure compatibility with most of today's PC software, and two boards based on Texas Instruments' 340 μP series to meet the needs of both today's most ad-

EDN's PC All-Stars

PC Mouse II

Mouse Systems Corp, 47505 Seabridge Dr, Fremont, CA 94538. (415) 656-1117. FAX (415) 770-1924.
Circle No. 676

STATS:
TRACKING TECHNOLOGY: Optical
INTERFACE: RS-232C (bus version available)
BUTTONS: 2
RESOLUTION: 200 counts/in. (hardware); 20 to 6400 counts/in. (with software)
POWER SUPPLY: no external supply needed

BIO: The PC Mouse II features full compatibility with Microsoft's mouse. It offers optical reliability and variable resolution through special driver software.

vanced software packages and future software products. The All-Star PC doesn't, however, use all three display cards at once. The Multisync Graphics Engine from NEC Technologies provides a single-card solution by combining VGA functions with a 34010-based graphics accelerator (**Fig 2**). NEC's card incorporates 1M byte of video RAM and 768k bytes of program RAM for the accelerator. The card's VGA section supports resolutions to 800×600 pixels. Its accelerator section generates a 1024×768-pixel image and displays as many as 256 colors at one time.

NEC supplies several software products with the board, including the direct graphics software standard (DGIS) and GSS*CGI (Graphic Software Systems' computer graphics interface), both developed by Graphic Software Systems (Beaverton, OR, (503) 641-2200). NEC also offers drivers for Microsoft Corp's Windows 286 and 386, drivers for Autodesk's Autocad 9 and 10, and an optional PC-Xview package, also developed by GSS, which transforms a PC equipped with the Multisync Graphics Engine into an X-Windows-based Unix terminal.

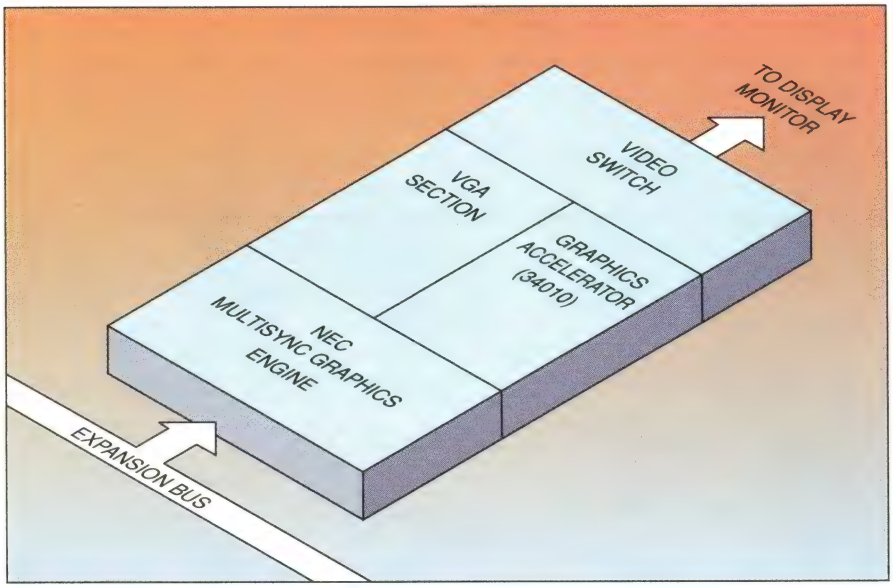


Fig 2—With a VGA controller and a graphics accelerator on one board, NEC's Multisync Graphics Engine provides multiple resources for display generation while consuming only one mother-board slot.

Speed problems rise again

During initial system-integration attempts at Cheetah International's R&D lab, the NEC Multisync Graphics Engine exhibited two particularly vexing problems. First, the VGA section wouldn't initialize properly more than half of the time. Second, the accelerator section didn't always draw vectors correctly during AutoCAD redraw operations. Cheetah's engineers and I suspected that the 80486's speed was causing these problems. As you recall, it wouldn't have been the first speed-related I/O problem for the All-Star PC Project. During the video initialization sequence (after turning on the power or resetting the PC), the Multisync Graphics Engine produced a double-sized cursor on the display, and the computer booted (as indicated by the integral power-on self-test display on the Cheetah Gold 425 mother board), but nothing else appeared on the PC's screen. The double-sized cursor indicated that the Multisync Graphics Engine's VGA section was improperly identifying the type of CRT monitor connected to the system.

This problem sometimes occurs with autoswitching VGA cards, and we felt that the speed of the 80486 code could cause a latent firmware bug to become a full-blown problem. We conferred with the card's designer at GSS and eventually obtained a new video BIOS ROM that fixed the problem. Chips and Technologies Inc (San Jose, CA, (408) 434-0600) designed the VGA chip on the Multisync Graphics Engine and also supplied the video BIOS. Because of the possibility of interaction between the VGA and mother-board BIOS ROMs, we discussed this problem with GSS (and thus, indirectly, with Chips and Technologies) and Award Software. Award also supplied a VGA BIOS ROM for the Chips and Technologies VGA controller chip, and that ROM cured the problem, too.

The undocumented nature of the PC/AT bus indirectly caused the Multisync Graphics Engine's 34010-related bug. Fortunately, it was easy to squash. IBM gave the PC/AT bus a handshake signal, called

I/O channel ready, so that slow I/O cards could stretch bus cycles. The Multisync Graphics Engine asserts this signal asynchronously (without reference to the bus clock). The asynchronous nature of the card's ready handshake sometimes threw the I/O bus state machine on the All-Star PC's prototype Cheetah Gold 425 mother board into a metastable state, a condition that appeared as misdrawn vectors. Ron Sartore at Cheetah quickly found and fixed this problem by adding a synchronizing latch to the state machine's I/O-channel-ready input.

The problems encountered with NEC's Multisync Graphics Engine illustrate the potential disadvantages of using any I/O card that combines two or more functions. If we had not been able to fix problems with the card's VGA section, we couldn't really have used the graphics accelerator portion except in a 2-monitor arrangement, a very unsatisfactory solution. However, the Multisync Graphics Engine now provides EDN's All-Star PC with an efficient combination of a VGA and an advanced graphics-display controller.

Two cards deliver more power

I also experimented with a 2-card graphics solution in the All-Star PC by teaming a VGA card with a 34020-based TIGA controller board (**Fig 3**). Because this design approach uses enough circuity for two pc boards, both the VGA and TIGA sections could include more capabilities than the corresponding sections on NEC's card. A VGA/NTSC recordable video card from US Video provides standard VGA functions. This card features a 16-bit bus interface for maximum performance. In addition, the board sports a 3-position switch that allows you to change its video timing from normal VGA frequencies to NTSC frequencies. When switched to NTSC, the video card generates a standard RS-170 color TV signal so you can display VGA graphics on standard TV monitors. You can

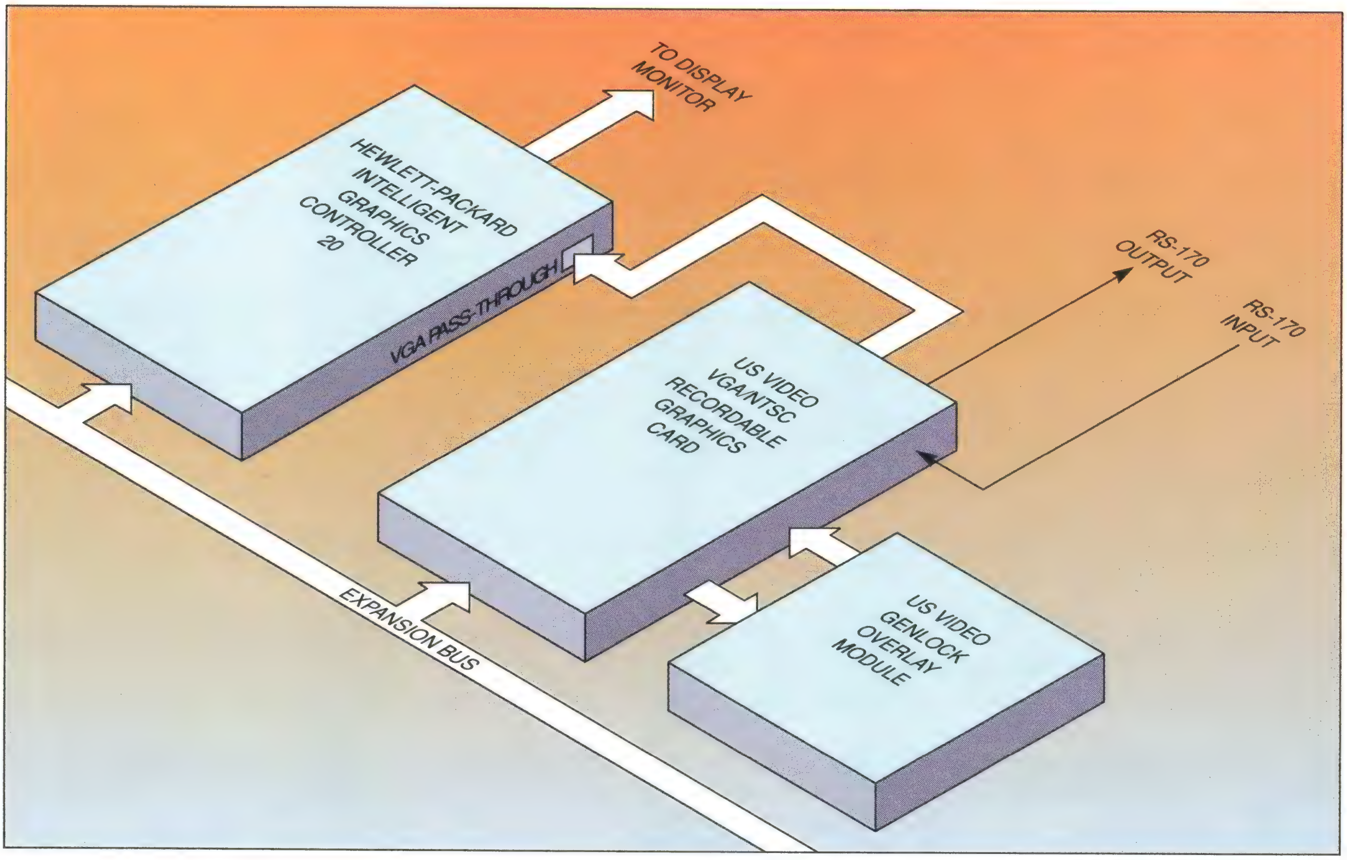

TO DISPLAY MONITOR
HEWLETT-PACKARD INTELLIGENT GRAPHICS CONTROLLER 20
VGA PASS-THROUGH
RS-170 OUTPUT
RS-170 INPUT
US VIDEO VGA/NTSC RECORDABLE GRAPHICS CARD
US VIDEO GENLOCK OVERLAY MODULE
EXPANSION BUS

Fig 3—Using two display cards, you can obtain vast improvements in PC graphics. In this version of the All-Star PC's graphics subsystem, a US Video VGA/NTSC recordable video card delivers PC-compatible displays with resolutions to 1024 × 768 pixels, and a Hewlett-Packard IGC 20 graphics accelerator provides high-speed, intelligent graphics.

also record this signal on any standard US videocassette recorder for later playback.

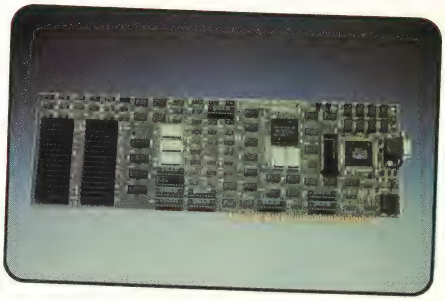
IBM's CGA card for the PC also had a video-output jack that could display a color picture on a standard TV, but with only 200 lines of resolution. US Video's NTSC recordable video card can display more than 400 lines on a conventional television monitor. (Note that most US TV sets cannot display VGA's full 480-line resolution.) With the addition of a daughter card, the US Video controller can synchronize the PC's graphics with an incoming video signal, a feature called genlock. Recordable VGA graphics with genlock capabilities help media moguls create dandy animated video productions, but the reason the All-Star PC has a US Video card is an engineering one. It's not merely a frivolous addition.

Engineering with videotape

Consider a test setup with a PC controlling the test apparatus and displaying the important test results using VGA graphics. The genlock/VGA video combination and a TV camera allow you to superimpose the test data on the image of your experiment and record the composite image on a VCR for later review. The superimposed test data would automatically be time-correlated with the recorded image of your experiment on the video tape. A T160 VHS cassette allows you to record eight hours of an unattended experiment, and you can review these results at your leisure. Like many engineers, I have conducted several experiments that required all-night stays at the environmental test chamber, just in case the prototype stopped working. If a design failed, I had to know

EDN's PC All-Stars **Multisync Graphics Engine**

NEC Technologies Inc, 1255 Michael Dr, Wood Dale, IL 60191.
(312) 860-9500.
Circle No. 677

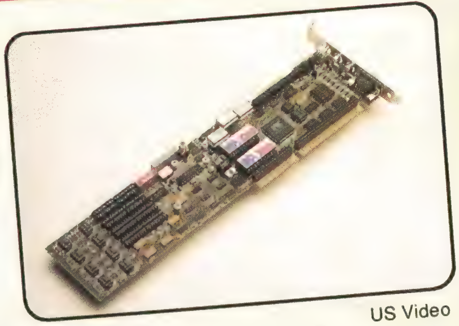

NEC Technologies Inc

STATS:
μP: Texas Instruments 34010, 50 MHz
MEMORY: 1M byte of video RAM; 768k bytes of program memory
VGA DISPLAY RESOLUTIONS: 640 × 480, 800 × 600
ADDITIONAL DISPLAY RESOLUTIONS: 1024 × 768
COLOR PALETTE: 256k colors, 256 displayable

BIO: The Multisync Graphics Engine combines the functions of a VGA display adapter and a graphics accelerator. The graphics-accelerator section is compatible with several PC graphics packages and standards including Windows and DGIS.

EDN's PC All-Stars **VGA/NTSC Recordable Graphics Card**

US Video, One Stamford Landing, 62 Southfield Ave,
Stamford, CT 06902. (203) 964-9000. FAX (203) 964-1824.
Circle No. 678


US Video

STATS:
BUS: IBM PC, PC/AT
OUTPUTS: VGA, NTSC RS-170
INPUT: RS-170
DISPLAY RESOLUTIONS: 640 × 480; 800 × 600; 1024 × 768
COLOR PALETTE: 256k colors, 16 or 256 displayable

BIO: US Video's VGA/NTSC recordable graphics card supports standard and enhanced VGA resolutions and generates standard RS-170 video signals for TV applications. An optional genlock overlay module allows the board to synchronize PC graphics with analog video.

when it failed and what the temperature was when the failure occurred. This video setup would have allowed me more pleasant evenings. You can also use this same videocamera/VGA combination to document assembly procedures or make training tapes.

US Video's VGA/NTSC recordable video card certainly enhances the capabilities of today's PC software, but some of today's and many future software products will require intelligent graphics processing. Hewlett-Packard supplied the All-Star PC with a 34020-based Intelligent Graphics Controller 20 (IGC 20) display card for just such high-end graphics needs. The IGC 20 incorporates 2M bytes of video RAM and 3M bytes of RAM for the card's operating program and for the graphics-display list, respectively. In this configuration, the IGC-20 can display 1280×1024- or 1024×768-pixel images with 256 colors.

The 32-bit 32020 μP and 5M bytes of memory consume the entire IGC 20, leaving no room for a VGA controller on the board. Instead, the IGC 20 accommodates an external VGA card via a pass-through connector. You connect the output of a VGA card to the IGC 20's pass-through input connector and then connect your monitor to the IGC 20's video-output connector. At power up, the IGC 20 links the pass-through and video-output connectors, passing any incoming video signals to the display. Only when you activate the IGC 20's TIGA functions does the card assume control of the video-output connector.

This configurability permitted experimentation with two different 2-board configurations. You can connect either the VGA/NTSC recordable video card or NEC's Multisync Graphics Engine to the IGC 20's pass-through input connector. Both of these configurations provide VGA functions, and the second configuration jams two different graphics accelerators into the All-Star PC. The IGC 20 conveys the Multisync Graphics Engine's high-resolution video signals just as easily as the VGA signals. Although you can only use one accelerator at a time, the flexibility of the pass-through arrangement is apparent.

Balancing cost and resolution

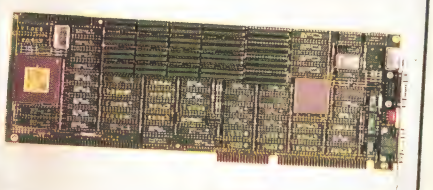
The All-Star PC requires a very capable display monitor because it incorporates so much graphics-processing power. Because PCs now support several different display formats (CGA, EGA, and VGA, just to name a few) and because of the addition of a 1024×768-pixel resolution to this display menagerie, only a multifrequency monitor could meet the All-Star PC's display requirements. I tried three 16-in. multifrequency monitors, which all worked well. Once again, however, selections were based on preference rather than specifications. I picked the NEC Multisync 4D monitor because I like the way it displays text and I relish its simple operating controls. The Multisync 4D displays images with resolutions to 1024×768 pixels, and because it is an analog monitor, it can display a continuous range of colors.

Note that the Multisync 4D can't display the output of the IGC 20 in its highest resolution. You may wonder why the All-Star PC uses the IGC 20 at less than its maximum resolution. First, there's a big price jump between monitors that can display 1024×768-pixel images and monitors that operate at higher

EDN's PC All-Stars **Intelligent Graphics Controller 20**

Hewlett-Packard Co, 19310
Pruneridge Ave, Cupertino, CA
95014. (800) 752-0900.
Circle No. 679

STATS:
μP: Texas Instruments 34020
MEMORY: 2M bytes of video RAM, 3M bytes of program memory
STANDARD DISPLAY SUPPORT: pass-through connector
DISPLAY RESOLUTIONS: 1024×768, 1280×1024
COLOR PALETTE: 16.7M colors, 256 displayable



Hewlett-Packard Co

BIO: Hewlett-Packard's Intelligent Graphics Controller 20 card employs a 32-bit graphics μP to accelerate PC graphics and is compatible with a variety of PC graphics standards including TIGA and DGIS.

EDN's PC All-Stars **Multisync 4D CRT Display Monitor**

NEC Technologies Inc, 1255 Michael Dr, Wood Dale, IL 60191.
(312) 860-9500.
Circle No. 680

STATS:
RESOLUTION: 1024×768 pixels
HORIZONTAL FREQUENCY: 31.5 to 57 kHz
VERTICAL FREQUENCY: 50 to 90 Hz
VIDEO INPUTS: analog
SCREEN SIZE: 16 in., nonglare
DOT PITCH: 0.28 mm

BIO: NEC's Multisync 4D display monitor provides high-resolution graphics while consuming a reasonable amount of desk space. An integral μP synchronizes the display to various video sweep rates and adjusts the picture size for each display mode according to selections preset by the user.

resolutions. Those higher-resolution monitors generally employ 19-in. CRTs and consume a tremendous amount of desk space. Furthermore, my experience with CAD and CAE systems, acquired as a design engineer at Cadnetix Corp (now Dazix) in Colorado, taught me that a display with 1024×768 pixels is perfectly adequate for CAD and CAE applications and for graphics-user interfaces.

The NEC Multisync 4D completes the All-Star PC's user interface and its complement of hardware components. It's time for the 7th-inning stretch. The last two articles in EDN's All-Star PC series will discuss the project's software entourage. **EDN**

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4. Mosley, J D, "VGA chip sets," *EDN*, March 17, 1988, pg 118.

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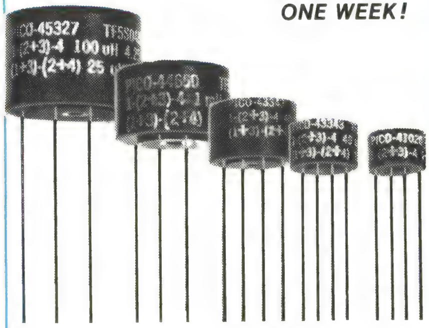

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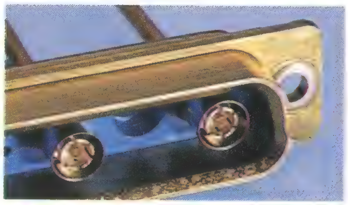

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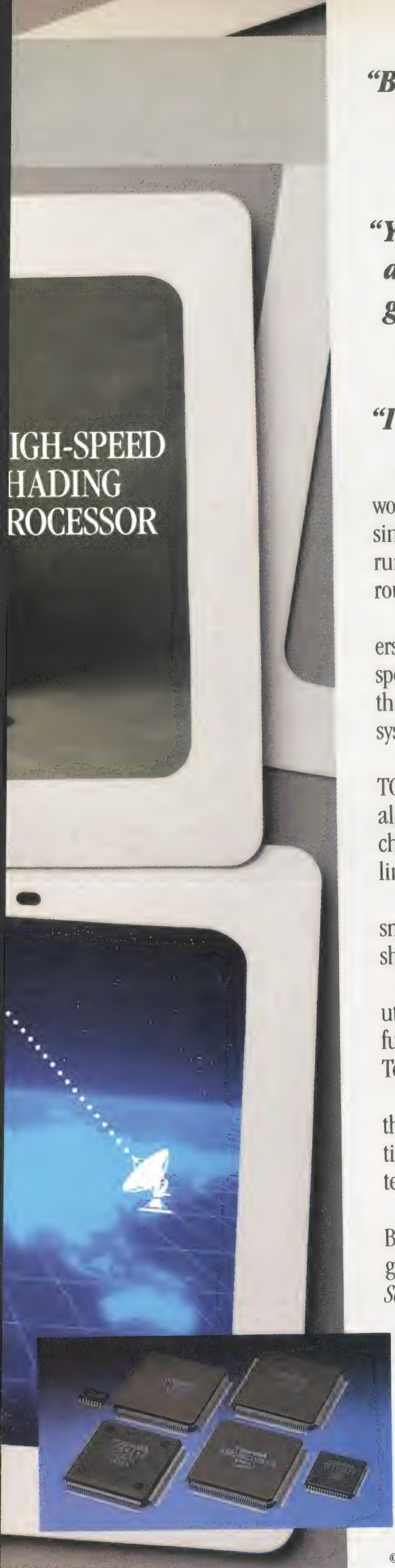

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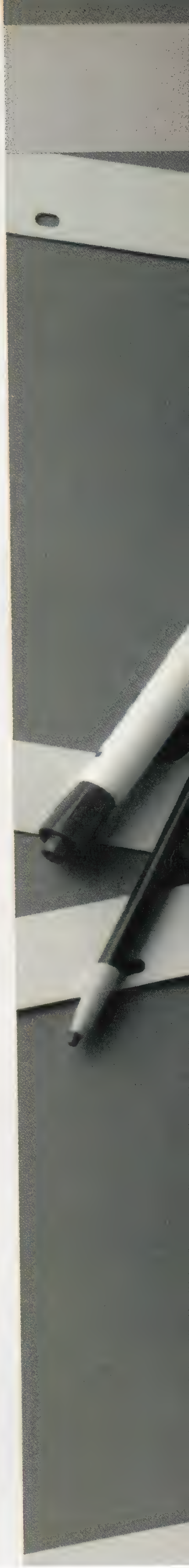

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CIRCLE NO. 75

Specific optimizations adapt C to single-chip µPs

The first part of this 2-part series contrasted how conventional C programs should work and how well single-chip µPs suit C. This part covers C extensions and optimizations tailored for specific single-chip µPs and includes detailed programming tips for writing tight C programs.

Charles H Small, *Senior Editor*

Far more interesting than the routine optimizations outlined in the first part of this series are optimizations and extensions to C that target a specific single-chip µP. Compiler designers have devised stratagems for compiling C code for common single-chip µPs, such as the 64180 and Z180, the 8051, and the 68HC11. These stratagems cover extensions, setting up pointers, taking advantage of µP-specific instructions, and altering C's execution model to accommodate specific single-chip µPs. Once you find a compiler that has the features you require, you can take advantage of detailed programming strategies and tips to help you tailor your C programs to the dictates of single-chip µPs.

Using a single-chip µP's special instructions is the hallmark of a hard-working compiler designer **(Fig 1)**. For example, Z-World's C compiler has several features that exploit unique features of the 64180 and Z180 single-chip µPs (both single-chip µPs have Z80 cores). The compiler supports the 64180/Z180's internal bank-switching mechanism by automatically inserting bank-switching macros into your program where needed. It also assembles a small root program, which is necessary for bank-switching, into each page of the single-chip µP's memory.

Z80 to the core

The company's 64180/Z180 compiler has several extensions, one of which is a special version of the *#asm* C preprocessor command called *#entry*. When you flag an interrupt routine with *#entry*, the compiler will generate code that saves all single-chip-µP registers upon entry and restores them upon exiting. The compiler also has a special preprocessor declaration, *#shared*, for variables that need the protection of a critical-code lockout.

In addition, the compiler speeds the execution of Boolean-logic operations, such as ANDs (*&&*) and ORs (‖), if they are operating on quantities such as FFxx$_{\text{HEX}}$ or xxFF$_{\text{HEX}}$. The compiler takes advantage of faster instructions for 8-bit operations on half of the 64180/Z180 single-chip µPs' 16-bit registers. Like many single-chip-µP C compilers, this compiler adds a *byte* data type for 8-bit math operations.

The company's 64180/Z180 compiler uses the 64180/Z180's special string-handling op codes for common C string-library routines and fast block-memory moves. It also uses the 64180's hardware-multiply facility.

Note that Z-World's compiler is one part of an integrated environment that operates much like Borland's

> *Using a single-chip μP's special instructions is the hallmark of a hard-working compiler designer.*

Turbo C or Microsoft's Quick C. But instead of producing code that runs on a personal computer, Z-World's compiler compiles directly into the company's ROM emulator, which plugs into your target system.

8051 follies

Some of the most powerful 8051 instructions are its bit operators. Therefore, as other 8051 compiler vendors have done, BSO/Tasking and Archimedes have added the *bit* data type to C as extensions. The compilers' local optimizers use the 8051's built-in Boolean processor to manipulate variables typed as *bit* **(Fig 2)**.

The companies' 8051 compilers also have extensions to C for assigning variables to the 8051's various memory spaces, such as *code, data, idata,* and *xdata*. These types let you fix your program elements as code, as data in internal RAM in the high or low page, or as external data—both directly addressed and banked. Each 8051 memory area has its own instructions and instruction-execution speeds. Thus, the location of a variable has an effect on your program's speed and size.

With Intermetric's 68HC11 compiler, you can consign program elements to the single-chip μP's on-board EEPROM.

Pointers are a unique and powerful feature of C. Using these single-chip-μP extensions, compilers can produce the shortest possible addressing sequences for pointers. For example, in an 8051, *char idat *idat* yields a 1-byte pointer, but *char xdat *idat* takes two bytes. Not all compilers use the same mechanism for assigning code and data to specific memory spaces and locations. Be sure that any compiler you choose can handle constructions such as *xdat *(*idat a[ ])(void);*. This statement sets up a pointer (*xdat*) to a jump table (*a*[ ]) containing pointers (*idat*) to the entry points of functions.

```
                                               main ()
                                                {
0100 A6 07      LDA     #$07                      i = 1 + 2 | 4   ;
0102 B7 2A      STA     $2A

0104 C6 20 00   LDA     $2000                     j++;
0107 4C         INCA
0108 C7 20 00   STA     $2000

010B 3C 2A      INC     $2A                       i++;

010D C6 20 00   LDA     $2000                     j = j & 0x7f;
0110 A4 7F      AND     #$7F
0112 C7 20 00   STA     $2000

0115 1F 2A      BCLR   7,$2A                      i = i & 0x7f;

0117 C6 20 00   LDA     $2000                     j = j & 0x20;
011A A4 20      AND     #$20
011C C7 20 00   STA     $2000

011F B6 2A      LDA     $2A                       i = i & 0x20;
0121 A4 20      AND     #$20
0123 B7 2A      STA     $2A

0125 81         RTS                             }
```

Fig 1—The 6805, like all members *of the 68xx family, has a special set of instructions for operations in the lowest memory page. In these code fragments, the C compiler has generated different instructions for* ***i*** *and* ***j****, which are below and above location 255, respectively. (Listing courtesy Byte Craft)*

Although C handles pointers, it doesn't know about interrupt vectors. BSO/Tasking's 8051 C compiler, on the other hand, has an extension to C that lets you link an interrupt to a particular interrupt routine.

Missing instructions

Several 8051 instructions have no corresponding C operators. For instance, the roll instruction, *RL*, has no equivalent in C. The BSO/Tasking 8051 compiler contains several built-in functions you can use as normal library function calls but which really expand into in-line code. For example, the *_roll* function, rotates the contents of a character object two positions **(Fig 3)**.

The Byte Craft C6805 C compiler for the 6805 μP uses artificial-intelligence "rules" to optimize programs. These optimizations range from simple constant-lofting to manipulating the intermediate code to reduce either its size or temporary-storage requirements. The company states that these expert-system rules are formal descriptions of 6805 programming experience. Some of the rules come from in-house experience, others from the company's customers.

About one third of the rules are specific to the 6805. For example, the compiler's code generator knows that branches are shorter than jumps and that register transfers are quicker and shorter than loads. It also knows that arguments to some instructions may have 0, 1, or 2 bytes. Consequently, the code generator tries

```
bit bitvar1, bitvar2, bitvar3;

bitvar1 = bitvar2 & !bitvar3;
bitvar3 = 0;
if (bitvar2)


MOV  C,bitvar2
ANL  C,/bitvar3
MOV  bitvar1,C
CLR  bitvar3
JNB  bitvar2,LABEL
```

Fig 2—Extensions to C let you *use the 8051's powerful bit operators. (Listing courtesy Archimedes)*

to use the fastest and most compact instructions. For example, it uses the 6805's bit instructions. And for operations using offsets from the index register, the compiler first checks the offset value and then employs the appropriate indexed instructions. Some C compilers would use a worst-case instruction indiscriminately.

Okapi's 68HC11 C compiler applies various assembly-code templates to the results, or "expression trees," of its analysis of your C program. These templates let the compiler apply different assembly-language sequences to the same C construct, depending on the context. For example, in the 68HC11, an assembly-language programmer can often use registers A and B in chained calculation to store intermediate results. Using templates, the compiler can treat registers A and B as separate registers in some instances and as a single 16-bit accumulator in others.

Avocet's 64180/Z180 C compiler substitutes a clear instruction for moving a zero into a register. If a program pushes an argument onto the stack and immediately pops it, the compiler will use the Z80 exchange instruction instead of pushes and pops.

```
void
main(void)
{
        unsigned char      c;

        c = _rol( c, 2 );
}


; 8051 C Compiler  Version 1.0  Serial # 00000000
  (c) 1990 Tasking BV
; options: -Ms -s
$CASE
        NAME  rol2
; rol2.c        1   void
; rol2.c        2   main(void)
; rol2.c        3   {
        PUBLIC        _main
C51_DA        SEGMENT      DATA
        RSEG  C51_DA
_1:     DS    1
C51_PR        SEGMENT      CODE
        RSEG  C51_PR
_main:
        USING 0
; rol2.c        4            unsigned char     c;
; rol2.c        5
; rol2.c        6            c = _rol( c, 2 );
        MOV   A,_1
        RL    A
        RL    A
        MOV   _1,A
; rol2.c        7   }
        RET


        END
```

***Fig 3—One way to make specialized 8051 instructions** available to a C programmer is to have C functions that compile into macros. This example ferrets out the 8051 roll (RL) instruction. (Listing courtesy BSO/Tasking)*

Note that not all single-chip μPs have special bit-field instructions. For the 64180/Z180 single-chip μPs, you might as well consign each bit variable to its own location rather than try to compress them all into one location. For these devices, the code necessary to access a bit in a bit field takes up more room than you save by using the bit field in the first place.

Altering C

Optimizing C compilers can alter C's execution model to accommodate single-chip μPs. For example, Archimedes's compiler allocates all 8051 data statically instead of using temporary variables on the stack. Function parameters and variables go in fixed locations in memory. When the program no longer needs a certain location, other parameters or variables can use that location. Thus, C programs can run on the 8051 without costly stack operations and without consuming any unnecessary RAM.

The company charges its linker, rather than its compiler, with assigning locations to variables. The reason the linker takes care of allocating variables is that only the linker can detect recursive calls, so only it can save variables that are still active. Thus, recursive programs can often use fixed variables. Recursion still demands some popping and pushing on the stack. Therefore, the recursive parts of the program have to run slower than the typical nonrecursive parts of the program.

The Archimedes 8051 compiler keeps function-call return addresses on the 8051's internal stack for maximum speed. However, the 8051's small internal-stack size limits allowable function nesting. If your program needs deeper nesting, setting a compiler "switch" (activating or disabling a compiler option) enables the compiler to swap return addresses from internal RAM to external RAM instead of overwriting the stack. If you keep the function-nesting depth below this threshold, function calls will still be fast. Remember, that in a C program, the 8051's stack has many uses, including math support, expression evaluations, storing interrupt returns, as well as recursion. Not corrupting a stack that performs many different functions is a challenging task for the compiler designer.

Z-World's 64180/Z180 compiler has a number of nonstandard preprocessor commands. For example, you can select different schemes for implementing the stack pointer. Also, the compiler has a C extension called a "subfunction." This extension lets you define a simple

Optimizing C compilers can alter C's execution model to accommodate single-chip µPs.

operation as a subfunction and then call it from within another function. This compiler, in effect, gives you optional manual control over common-subexpression optimization.

You cannot call one Z-World subfunction from within another subfunction because the subfunction call compiles to only a simple call and return and does not use the complete, elaborate, C function-calling conventions. Using subfunctions, you can compress your program's size at the expense of the added calls and returns.

An efficient function-call mechanism is crucial to the speed of any C system. With statically allocated local variables, functions require no complex entry sequences. By using registers efficiently, the compiler also saves a few precious bytes. In addition, a compiler can speed interrupt handling if it saves only the registers that an interrupt routine is going to use (**Fig 4**).

For a program to have some of the advantages of static data but retain re-entrancy, the Z-World 64180/Z180 compiler supports a *register* data type. The compiler really assigns each *register* item to a 16-bit static memory location, not a µP register. To retain re-entrancy, the compiler saves all the *register* locations on the stack upon function entry and restores them from the stack upon exit. This scheme guarantees that the function can call itself, or be called from a higher-priority interrupt routine, while it's executing. The scheme, yet another deviation from C's execution model, protects the function's current state because the higher-priority function saves and restores all *register* variables.

Note that in the case of a pre-emptive, multitasking system, this scheme could fail if two different tasks use the routine. In this case, you must use true "automatic" variables.

```
interrupt void timer(void)
     {
              P0.1 =0;/* Pulse prot low */
              P0.1 =1;/* And restore */
     }


timer:
     CLR     P0.1
     SETB    P0.1
     RETI
```

***Fig 4—In this example, an 8051 compiler** has decided it doesn't have to save any registers when jumping to an interrupt routine. (Listing courtesy Archimedes)*

The preceding examples should have driven the point home that you cannot just blindly write C programs for a single-chip µP. Even the most powerful optimizing compiler, with an infinite bag of tricks, cannot correct a bad algorithm. Nor can a fast processor make up for a bad program design. In these cases, the most you can hope for from a compiler is that you'll produce your bad program in record time. Never forget Small's Second Law of Software: "You can write really bad code in any language."

Accumulated wisdom

Some experienced C users would advise newcomers to simply get more memory if they're getting a compiler. Other, more helpful, gurus could provide a useful service to tyros. Only experienced C programmers could rate a compiler's C extensions, function library, and support for essential ANSI C enhancements such as *function prototyping*. They could also examine how each compiler's designer adapted C's basic execution model to the peculiarities of your single-chip µP. Take advantage of the accumulated wisdom of these programmers when choosing a C compiler for a single-chip µP. Also, Z-World can give you a C test program that the company claims will give any optimizing compiler a real workout.

A single test of your compiler's ability is only the beginning. You must always look at the assembly-language output of your compiler for each program you write. No matter how clean your program looks in C, you need to see how it looks to the single-chip µP. Here, you're probably on your own. Compiler vendors don't provide you with examples of how their compilers digest C programs.

C gurus won't help you either. Because gurus make a point of honor of writing as much of their programs as possible in C, they seldom soil their hands with assembly language. Many of them take pride in their ability to boil a C program down to a minimal, virtually unreadable form. They justify these C clots on the grounds that they are small and compact after compilation, too. Such may not be the case.

Innocently invoking a perfectly ordinary C operation could balloon your code unnecessarily. Some C constructs generate good code, some go supernova. For example, array indexes that aren't a power of 2 generate horrendous code compared with that generated by power-of-2 indexes. Multiplication is very costly in most single-chip µPs. One of C's specialties is pointers, but some single-chip µPs, such as the 8051, don't handle pointers efficiently.

Note that the assembly-language output of some compilers is easier to read than others. Most compilers assign nonsense names, such as V.1, V.2, V.3, to variables in their assembly-language output. They assign these names within functions during compilation so that a function can have private use of the same name used in other, different functions.

This practice makes the assembly language difficult to understand. Even if you track down the compiler's name for the variable in the assembly code it produces, that name could change with every minor recompilation. Some compilers keep your original name but add a suffix when necessary for privacy.

From choosing to using

Software engineers have already solved many common programming problems. A day or two spent going through journals and magazines can often save you considerable development time, execution time, and code space. The following is a collection of programming tips.

Isolate your source code into modules and check the size of each module after compiling. That way, you'll be alert to any module that has become disproportionately large.

If you use C in a disciplined way, you can write optimal programs. For example, in almost all C compilers, the pre- and post-increment operators, + + and – –, inform the compiler that it can use the processor's fast incrementing and decrementing instructions. Using these instructions instead of an add routine results in several times faster and smaller code, if your single-chip µP has such instructions.

C evaluates compound logical expressions for only as long as necessary to determine the final result. Putting test elements known to evaluate faster than the other elements in the test expression first often obviates executing the rest of the expression needlessly. C stops testing as soon as an AND element tests false or an OR element tests true.

You should avoid using the C ellipses construction, "...", for passing a variable number of arguments to a function. Using this construction hinders the optimizer because the function's behavior is undefined. If you don't use ellipses, the compiler can bypass the stack if the fixed number of arguments fits in available registers. With the ellipses construction, the compiler has no idea how many registers it might need to pass parameters and, hence, has no choice but to pass them on the stack.

ANSI C allows—but does not require—you to specify types and numbers of arguments. Take advantage of these options. Otherwise the compiler can promote types—for example, an 8-bit to a 16-bit datum—whenever it feels like doing so.

To avoid a penalty in code size and speed, use static data variables wherever possible. For the 64180/Z180 single-chip µPs, accessing static integer data requires only three bytes of code and 15 clock cycles. Accessing integer data on the stack requires six to eight bytes and 28 to 36 clock cycles. Also, avoid 32-bit operations with an 8051.

Use the smallest memory model possible. For example, Z-World's "compact mode" can save space at the expense of clock cycles. In the compact mode, the compiler calls a single copy of a repeatedly used test rather than writing it inline each time it's used. Further, accessing variables in memory consumes large amounts of time and space. Using the smallest memory model possible and the fastest-access variables in critical places is crucial. Archimedes compiler for the 68HC11 lets you declare variables in the single-chip µP's fast zero-page memory.

For large arrays, if most of the values fit into a smaller data type but some exceptional values exist, consider using the small data type for the bulk of the array and then testing for those exceptional, larger values.

Watch out for slow instructions in your program's critical path. For example, the 8051 has no support for signed math or the manipulation of variables other than *char* and *bit* variables. So even simple math on data types other than these executes more slowly.

Bit fields conserve RAM space and create clear data structures, but they're typically slower than arrays or *bit* variable types. For example, one bit variable of a set of 16 Boolean bit variables in a bit field will have a slower access time than one bit (in an otherwise unused byte) in an array of 16 *char*s. However, in the 8051, which has hardware for manipulating bit variables, access is an order of magnitude faster for a bit variable than for a bit field.

The C preprocessor does basic math operations on constants, thus saving time and space at runtime. Avoid interspersing constants with variables in compound expressions so that the preprocessor can recognize groups of constants and combine them. For exam-

An efficient function-call mechanism is crucial to the speed of any C system.

ple, using $j = i + k + (CONST1 + CONST2)$ rather than $j = i + CONST1 + k + CONST2$ saves you one out of three calls to the *add* routine at runtime. You don't need to sacrifice your program's readability by combining constants into subconstants when the C preprocessor will do it for you.

Function calls and loops

Each function-calling procedure costs you a fixed overhead plus a roughly linear time increment for each parameter a calling routine passes to a called routine. Loops require extra comparisons for their iteration counters. By unrolling function calls and loops into straight-line code, you can trade increased speed for increased code size. For example, the Archimedes *-s* optimize-for-speed compiler switch unrolls function calls automatically, thus letting you maintain the readability of your code. Because macros have no call overhead, rewriting short functions as macros can also save time.

Use C's *pragma* directive to gather up all nonANSI C extensions, so you can port your code to C compilers that don't have the extensions. For example, the BSO/Tasking 8051 compiler has a *pragma* command called *vector/novector* to control generating save/restore code for interrupt handling. If an interrupt-service routine does only internal data accesses, your main program need not save the 8051 data pointer. By specifying *pragma novector*, you must supply your own register save/restore handler, which could be smaller than the compiler's. A smaller interrupt handler, in turn, lowers interrupt latency.

One caveat concerning optimizers: You'll need the highest grade of cross debugger to handle optimized single-chip-μP programs. To the extent that an optimizer rearranges your code, it can also fool a symbolic debugger that's trying to correlate what you have written in C with what is actually running on your target system. Therefore, some compiler vendors advise that you debug your code with the optimizer turned off and reserve optimizing as the last step.

This dictum betrays the mind set of the conventional computer scientist. Remember that all conventional software-development tools ignore both time and code size. That is, computer scientists advocate writing high-level code, which is deliberately divorced from the processor's physical reality, into bottomless files. A C source program provides not a clue of its actual size or speed in your target system. High-level-language programmers accept this situation as normal. But there's something Kafkaesque about writing a program, which should, after all, completely and determin-

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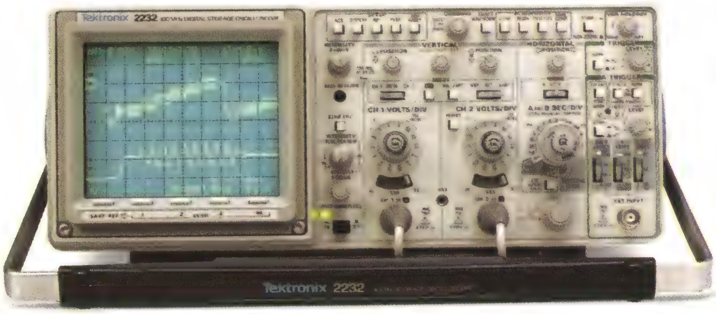

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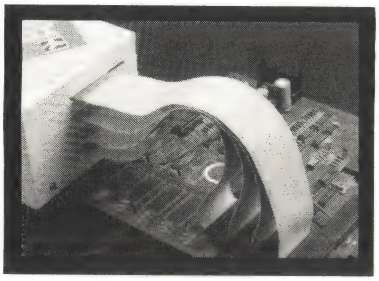

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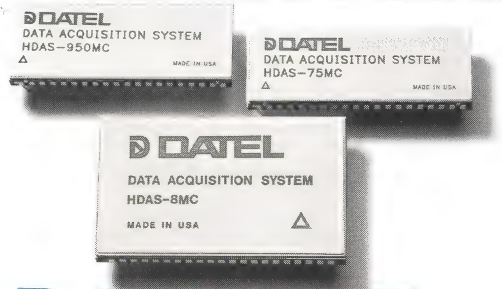

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Reference

1. Kernighan, Brian W and Dennis M Ritchie, *The C Programming Language, Second Edition*, Prentice Hall, Englewood Cliffs, NJ, 1988.

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CIRCLE NO. 108

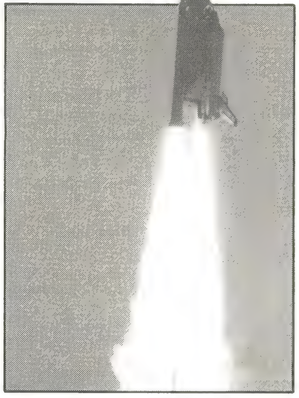
In 1979, Evelyn Ashford breaks 11 sec. in the 100-m dash for the 1st time…

and EDN takes 1st place in readership.

In 1980, the first-ever Chinese Olympic team attends the Winter Games…

and EDN wins 1st place in readership.

In 1981, the Columbia makes the first space shuttle flight…

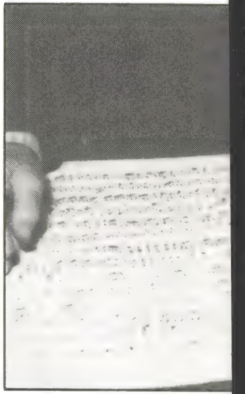


and EDN soars – finishing 1st in readership.

In 1982, Lady Diana, Princess of Wales, has her first child…

and EDN reigns as 1st in readership.

In 1983, the first symp written by Mozart (at nine) is discovered…



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Sipex Corporation	#1	4
Kyocera Northwest, Inc.	#1	NOT INCL.

CUMULATIVE WINS –
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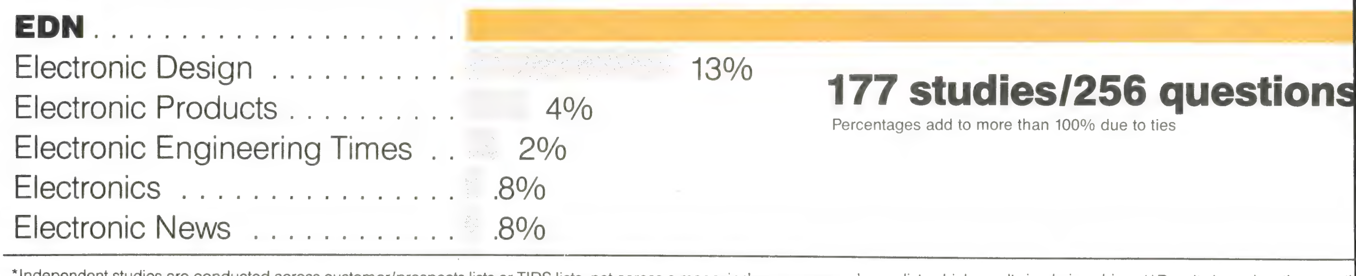

177 studies/256 questions

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*Independent studies are conducted across customer/prospects lists or TIDS lists, not across a magazine's or newspaper's own list, which results in obvious bias. **Results based on the questi

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and EDN is elected 1st in readership.

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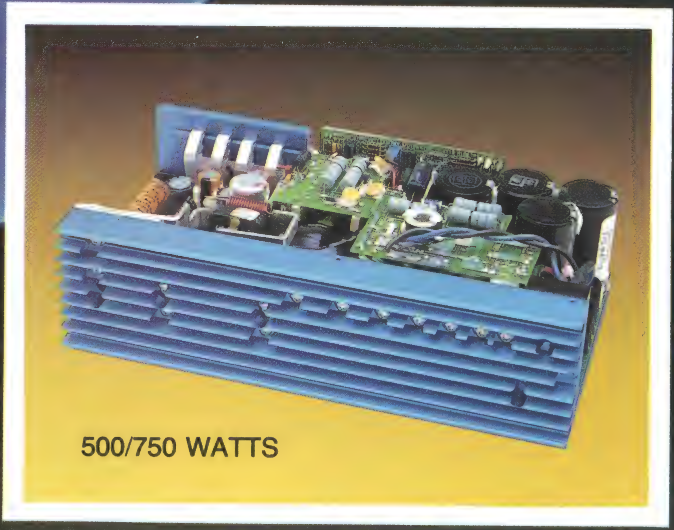

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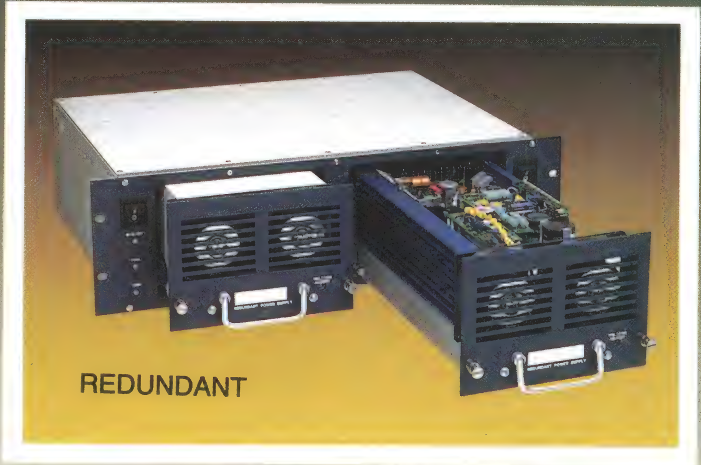

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CIRCLE NO. 109

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Most standard analog ICs leave something to be desired.

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# of what

You're looking for an edge. Through higher integration. Or performance improvements. Or unique packaging options. Things you've always wanted from standard analog products. But couldn't get.

Until now.

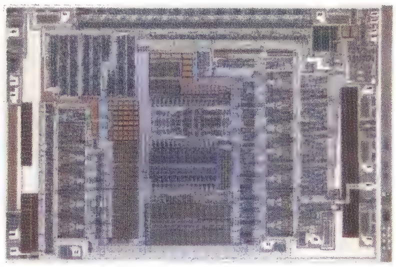
Because now there's semi-standard…a new way of thinking about analog design. One that gives you some of the rewards of analog ASIC, without many of the risks. Because you start with a standard product. If that's all you need, fine.

But if you want more—more drive current, more efficient space utilization, more system performance—semi-standard can give you that. In very little time. With minimal risk. In CMOS or bipolar processes.

Utilizing our proven ASIC tool set and design methodologies, we can enhance your standard solution by changing the functionality or performance characteristics. Or by tightening electrical, environmental or unique quality specifications. Or simply by modifying your packaging to optimize your system's requirements. And give you working bipolar prototypes in as little as 6 weeks, CMOS in as little as 12. Consider the possibilities.

The Lower, The Better.

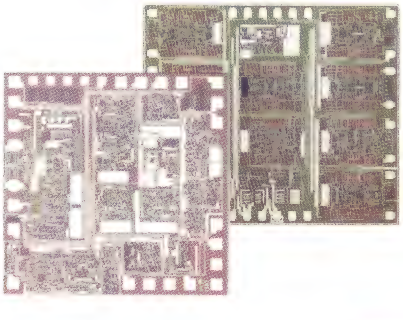
When one of our customers received a request from one of the major RBOCs to supply a telephone line equalizer with a very low group delay, we simulated the condition and simply re-wired the building blocks of one of our standard CMOS products. And delivered the goods, in less than 3 months.



standard: much more you need.

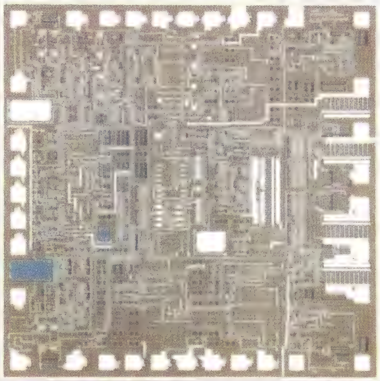
The Tighter, The Better.

By quickly and easily adding a unique trim capability to one of our standard hard disk drive servo products, we delivered a much tighter voltage reference and satisfied a major customer's critical power fail detect requirement. On time. On budget. Giving him a real competitive advantage. Responding to a number of customers' immediate needs, we also solved a system yield problem through tighter pulse pairing. By adding trim capability to our standard ML 8464C pulse detector, we were able to raise the performance specs by 200% and quickly solve their application problem.



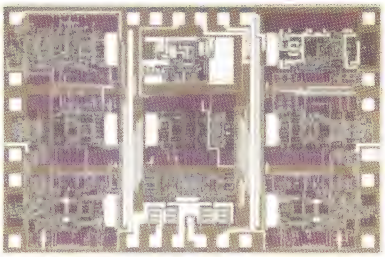
The Fewer, The Better.

When a major military supplier asked us to help solve a space problem on an advanced military radio, we used our FB 3490 tile array and existing macros to combine three 100KHz PWM controllers onto a single chip, in a single compact package. Quickly turning a standard answer into a small wonder.



The Smaller, The Better.

After evaluating our ML4621 Fiber Optic Inter-Repeater Link quantizer, three different networking companies asked us to develop smaller, lower power versions of our standard offering. The result? Two new versions, in TTL and ECL, each optimized for a particular interface, with lower pin counts and power consumption.



Micro Linear

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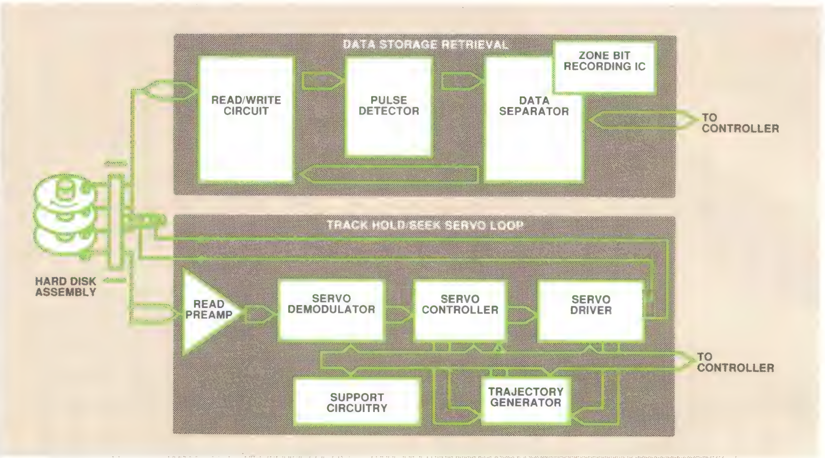
NOTES FOR DISK DRIVE DESIGNERS

How to design a strategic advantage into your next disk drive.

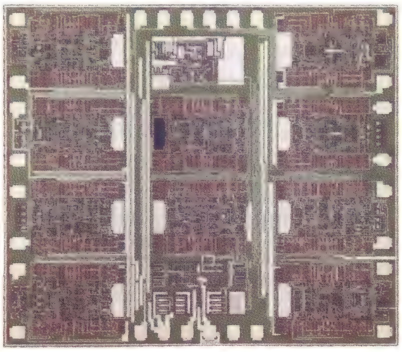


Micro Linear's full set of HDD ICs support both dedicated and embedded servo disk drives with read/write preamps, pulse detectors, phase locked oscillators and 8-bit data converters.

In the disk drive business, time to market is everything. Yet you can't be satisfied with standard read/write and servo control solutions.

What you need is semi-standard. Products with higher performance. Higher integration. Or increased functionality. That you can get in time to capitalize on narrow windows of opportunity. With a minimal amount of risk.

Semi-standard solutions like our ML8464C pulse detector, the first chip to offer a +/-1 nanosecond pulse pairing performance advantage, reducing bit error rates and increasing yields. Or our ML4041/4042 pulse detectors that combine 1 ns pulse pairing with $2\,\mu s$ write-to-read recovery in the industry-standard footprint.



Semi-standard solutions like the ML 4401 Servo Demodulator are based on Micro Linear's tile array technology, allowing modification of functional blocks to gain a competitive edge.

Or our ML4400 Chip Set that provides a highly integrated solution for fast-access, high TPI dedicated servo systems. It's a standard, off-the-shelf solution that's been designed with our bipolar tile-arrays. So you can start with our standard solution or modify the functional blocks to gain a competitive edge. And get working prototypes in as little as 6 weeks.

Got a high data rate drive that you want to race to market? Our new ML4025 data separator runs up to 33MB/s and is the only chip to support both RLL (1,7) and RLL (2,7) codes. Add constant density recording capability with our ML4417/4427 ZBR™ chip and you can achieve storage density advantages, with a VCO that operates over a 4:1 range up to 100 MHz.

You can even specify custom packaging options on any HDD product to satisfy critical on-board space requirements.

Want to know more about how you can gain a competitive advantage on your next drive? Just call (408) 433-5200, ext. 403, or write to:

Micro Linear
Dept. HDD
2092 Concourse Drive
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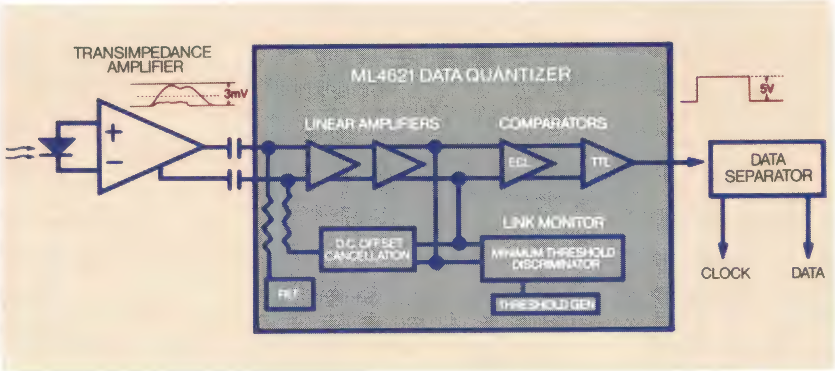
NOTES FOR ANALOG SYSTEMS DESIGNERS

Now there's a high performance single-chip solution for quantizing fiber optic signals.



ML 4621 converts Low Level Pulses from a PIN Diode Preamp into Clean Digital Signals.

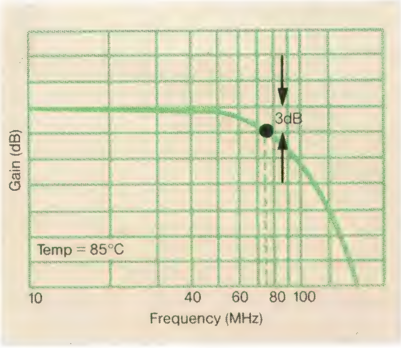
Micro Linear's ML4621 is the first complete solution for converting low-level analog pulses from a fiber optic PIN diode preamp to digital signals, enabling you to interface with the clock recovery circuit.

The ML4621 is a highly integrated high performance solution for many different types of fiber optic receivers, including IEEE 802.3 and IEEE 802.5 Local Area Networks.

High Frequency Design Made Easy

The ML4621 contains all the necessary circuitry for quantizing signals at data rates up to 100Mbaud. The chip includes a high speed comparator, wide band amplifier, a link monitor and a DC offset cancelling circuit. The high level of integration greatly simplifies the design of a fiber optic receiver by eliminating multiple discrete devices.

The ML4621 data quantizer can accept a wide dynamic range of signal strengths at its input, up to 55 dB.



ML 4621's Wide Bandwidth makes it usable to 100 MBaud

The wide dynamic range means the ML4621 can be used where combinations of high and low voltage input levels might saturate less accommodating, discrete solutions. The quantizer's low noise voltage (25μV) makes it insignificant compared to other components.

Once your data signal has gone through two cascaded stages of wideband (50MHz) gain amplification, you can choose between either a single +5V TTL comparator, or a +5V or −5.2V ECL comparator to interface with other blocks.

For minimum use of board space, two other versions, the ML4622 and ML4623, are available in smaller packages. One has only TTL outputs and the other has only ECL outputs.

Built-In Link Monitor

A user adjustable link monitor prevents incorrect data from being passed by disabling data outputs when incoming signals fall below externally set threshold levels. The circuit also transmits a status signal to the system.

Semi-Standard Versions

The ML4621 family is developed on Micro Linear's family of bipolar tile arrays. It allows easy customization to your specific applications, including the addition of blocks, such as a Fiber Optic LED driver, or a transimpedance amplifier, or changes in I/O and other packaging options.

Call Or Write For More Information

If you would like more information on the ML4621 fiber optic data quantizer, or on Micro Linear's complete line of linear devices, call (408) 433-5200, extension 900. Or write:

Micro Linear
Department Q4
2092 Concourse Drive
San Jose, CA 95131

Micro Linear

NOTES FOR POWER SUPPLY DESIGNERS

Now you have a choice for your power supply controller.

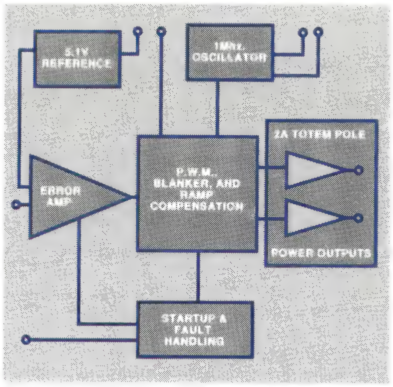
Standard devices for maximum performance.

1. Introducing three new single-chip Switch Mode Power Supply controllers that save space, money and time.

The new 16-pin ML4825 and ML4823 are improved pin-compatible replacements for the UC1825 and UC1823. A third new controller, the ML4809, is packed with extra features and functions for better stability, easier starting and synchronization.

PART TYPE	SOFT START RESET	UNDER-VOLTAGE OUTPUT STATE	COMPARATOR TO OUTPUT DELAY
ML4823 ML4825	COMPLETE	LOW	40 nS
UC1823 UC1825	PARTIAL	FLOAT	50 nS

Micro Linear/Unitrode Comparison



Micro Linear PWM Controllers Provide Maximum Performance

The ML4809 starts with all the features of the ML4825, then adds even more:

Synchronization:
- separate clock I/O pins
- wide dynamic range VCO
- toggle flip-flop output and preset inputs

Stability:
- on-chip programmable ramp compensation
- blanker to reject turn-on spike
- completely independent error ramp

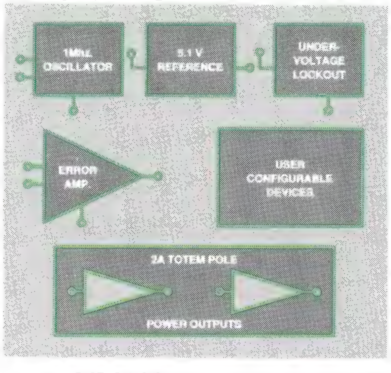
Start-up/Fault conditions:
- 7V hysteresis on under-voltage lockout
- full reset with programmable delay

If one of these new standard controllers doesn't meet your special high-frequency system needs, Micro Linear can provide a semi-standard part to your specific applications.

Semi-Standard devices for maximum flexibility.

2. Announcing the new FB3480, the first array specifically designed for high frequency Switch Mode Power Supply applications.

The FB3480 technology allows both Standard and Semi-Standard SMPS controllers to be quickly and easily developed starting from the same piece of silicon. This array contains crafted high performance "core cells" optimized to perform all the standard functions found in all PWM controllers. In addition a large area of uncommitted components on the chip can be configured to your specifications using Micro Linear's library of "soft macros." These macros implement a full complement of logic, comparator and other functions which make your controller unique. This approach allows you to evaluate the performance of the standard products then to customize a unique solution with a minimum of cost and effort, without sacrificing performance.



ML3480 Array Enables Easy Custom Design

For more information on the new single-chip standard and semi-standard SMPS controllers from Micro Linear, call (408) 433-5200, ext. 900.

Or write:
Micro Linear, Dept. PWM
2092 Concourse Drive
San Jose, CA 95131

Micro Linear

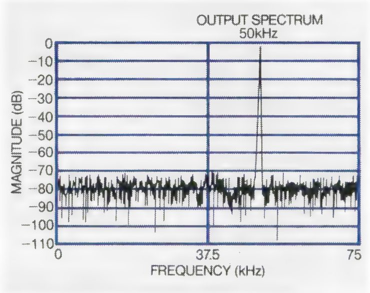
NOTES FOR ANALOG SYSTEMS DESIGNERS

New 8-bit A/D converters with sample and hold maintain accuracy at 50KHz.

The new ML2258 and ML2281 series from Micro Linear maintain true 8-bit accuracy while digitizing a 0V to 5V, 50KHz sine wave. This gives you near ideal signal-to-noise of 47dB. All devices come with either a double buffered parallel or serial digital interface. Yet, these devices are superior for interfacing to temperature, pressure and position transducers due to low cost and ease of use.

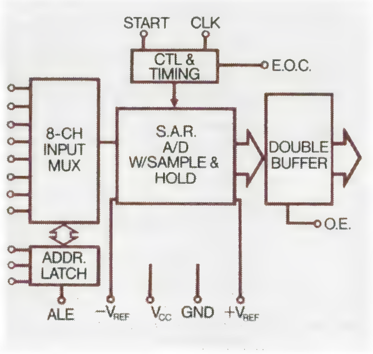
Dynamic Performance and 8-bit Guaranteed Accuracy

Dynamic performance and 6 microsecond conversion time make the ML2258 and ML2281 series ideal for signal processing as well as for digitizing sensors.



The FFT Plot of the ML2258 Converting a 50 KHz, 0 to 5V, Low Distortion Sine Wave Input.

Total unadjusted error in the ML2258 and ML2281 series is ±½ or ±1 LSB, which includes the sum of nonlinearity, full scale and zero scale errors. It is important to note that no full scale or zero adjust is required.



ML2258 Block Diagram

Designed for Ease of Use with a Choice of Analog Inputs

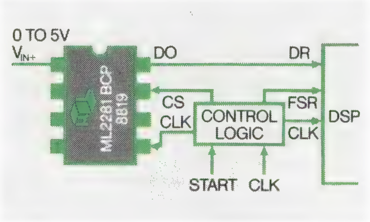
With all parameters guaranteed over the entire ambient temperature range, as well as ±10% tolerance of the single 5V power supply, the ML2258 and ML2281 series are designed for ease of use. Stable and repeatable conversions result from a digital code uncertainty of 1 mV.

Greater design flexibility is allowed by the 0V to 5V analog input range operating either ratiometrically or with a voltage reference up to 5V. The inputs are protected for up to 25mA maximum per input.

Power dissipation overall is extremely low—less than 3mA.

Digital inputs and outputs are both TTL and CMOS compatible.

The ML2258 microprocessor-compatible 8-bit A/D converter with 8 analog inputs has a double-buffered three state output and latched and decoded multiplexer address inputs. It is available in both 28-pin DIP or PCC.



ML2281 Serial DSP Interface

The ML2281 series 8-bit serial I/O A/D converters provide a serial address of the 2, 4, or 8 analog inputs. ML2281 series DIP packages are 8, 14 or 20-pin configurations. In addition, the 8-input channel ML2288 is available in a 20-pin PCC. Prices start at only $2.95 each in 100 unit quantities.

Semi-Standard Options

Customized versions of both series of converters are available to incorporate alternate packages, different specifications or slightly modified functionality.

If you would like more information on the ML2258 or ML2281 series A/D converters, or on Micro Linear's complete range of linear devices, please call (408) 433-5200, extension 912, or write:

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Since, 1983, we've pioneered the use of analog ASIC methodologies to produce high-performance, high reliability analog products for a wide range of commercial and military applications including computer peripherals, instrumentation, telecommunications, data communications equipment and military systems. Yours could be next.

To find out, simply send us your design problem with all the critical performance parameters. Our applications engineers will quickly analyze your problem, evaluate the alternatives and give you our best recommendation.

We'll even give you a number of development cost options—ranging anywhere from a one-time NRE charge to waiving it in exchange for the rights to eventually offer your design as one of our standard products.

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Routing out signals troubleshoots LCA designs

Although you can use ASIC design-verification techniques, such as software simulation, with Xilinx LCA field-programmable gate arrays (FPGAs), these devices will also yield to traditional in-circuit methods.

John Rostykus, *Data I/O Corp*

Unlike conventional TTL and PLD designs, Xilinx LCA (logic-cell array) designs have significant portions of their circuitry buried within the device. Therefore, you can normally observe only a small percentage of the device's signals with your logic analyzer or oscilloscope at the device's external pins.

Attempting to debug your design using only the externally visible signals usually leads to several iterations of

- guessing which portion of your design is causing the error
- modifying your original design in an attempt to isolate this portion
- testing your modified design in circuit to verify if your guess was correct
- repeating these steps if the guess was incorrect.

This type of debugging is slow, tedious, and often unreliable. The problem is that you cannot observe enough details to isolate the improperly designed subcircuit.

Making your LCA design's internal circuitry more observable, which this article will show you how to do, will allow you to use the same techniques you use for debugging traditional TTL and PLD designs.

This alternative method entails routing out some of the LCA's internal signals to external pins for observation. In practice, this new method has its own set of problems, but you can overcome most of them with patience and methodical practices.

Fig 1 shows the basic steps involved, along with the iterative nature of the method. The number of signals you will have to route out depends upon your design's nature, the particular error, and the number of pins available for routing out. Sometimes, routing out a single signal may suffice, while other times you may have to route out several signals.

Route out details

To perform a route out, return to the Xact editor to edit the LCA's layout directly. You could go all the way back to the schematic level, but this method takes significantly more time because of the subsequent placement and routing steps. Also, formally documenting these route-out changes in the original schematic is not important because the changes are only temporary.

The first step is to locate the signals you want to observe. Given your knowledge of how the design operates, locate the internal signals that generate the external signals you observed functioning erroneously. Typically these internal signals include those of funda-

Making your LCA design's internal circuitry more observable will allow you to use the same techniques you use for debugging traditional TTL and PLD designs.

mental logic blocks in your design such as state-machine bits, counter bits, clock enables, and decodes. Selecting these fundamental signals helps minimize the number of times you must perform route out, assuming you will be looking for more than one bug.

You must now determine which pins in the design are most easily available for route out according to the following criteria: unused/unconnected pins, dedicated output pins, or, lastly, dedicated input and bidirectional pins that you can temporarily transform into output pins.

The first choice is to use an LCA pin not used in your design and not connected to other circuitry in your system. The second choice is to use an LCA pin that is an output pin in your original design and that you can temporarily change without adversely affecting the entire breadboarded system's operation. For example, a system-clock output may be a bad choice. The third, and worst, choice is to use an LCA pin that is an input, or bidirectional, pin in your original design. Use such a pin only as a last resort, because this choice requires disabling the driver in your prototype connected to this pin. Using input pins for route out is usually only feasible on breadboards where chips are often socketed and you can "lift" the corresponding driver's pin.

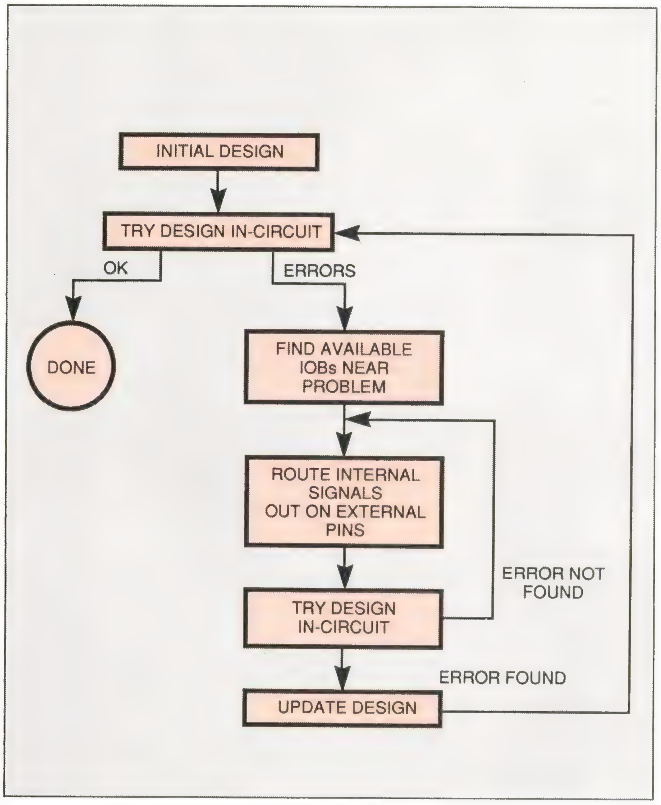


***Fig 1—This flowchart shows the various steps** of the route-out method. Plug the initial design into the target system and test it in circuit. By monitoring external pins on the device, you learn that your design is not behaving as expected. You must now infer which particular subsection of the design is not functioning properly. You then go back into the design editor and route out some signals, which may be causing the problem, to available external pins. Next, you monitor the circuit's performance, including the extra route-out signals. By performing enough route-out iterations, you can pinpoint the problem.*

Next, locate the complete routing paths, or "net," of selected signals in your routed LCA using the Xact editor. You will use this information to select among the available LCA pins.

The subsequent step is to choose a specific pin for each selected net by trading off the proximity of the pin to the selected net for the routing congestion between the pin in question and the selected net. In most cases, the best choice is the pin that is closest to the selected net. If the selected net is in the center of the LCA (not near any pin) or the net is equally close to more than one pin, the second criterion comes into play.

Current LCAs have a limited number of routing resources or "channels" for interconnecting the chips' elements, what their manufacturer calls configurable logic blocks (CLBs) and I/O blocks (IOBs). You will probably have already used most if not all of these channels. Routing congestion occurs when your existing routing uses all of the available channels in a particular region, such as between two adjacent CLBs. This congestion precludes routing an additional signal between such CLBs without modifying the existing routing. To simplify routing out your selected signal, choose the pin that has the least routing congestion, or conversely, the greatest number of available channels, in the region between the selected signal and the pin.

Once you have chosen a pin that is both near the selected signal and has the least routing congestion, the next step is to configure the pin as an output. Finally, you must route a new segment of the selected net to the route-out pin. This step can be as simple as letting the editor automatically route the net or as complex as rerouting several existing nets to make room for the new connection to the route-out pin. In most cases, after carefully selecting the route-out pin and considering existing routing congestion, the LCA editor will automatically route the net. However, in some cases it won't do so automatically.

In these cases, you are left with a couple of options.

pulse), DWNSTR (down start), or RDPLS (read pulse)—then it goes into the Read (01) state to read one bit of data. If C clock pulses continue coming in, it will remain in the Read state; if C clock pulses stop, it will return to the Refresh (00) state.

From the Refresh state, if a WRRAM (write RAM) request from the communication link comes in, the state machine changes to the Pre-Read (10) state for one cycle, followed immediately by a transition to the Write (11) state for one cycle. These transitions enable writing one bit to the 2-bit-wide RAM. The DRAM controller then returns immediately to the Refresh state.

Fig 3 is a schematic of the DRAM-control block. Inputs from the configuration-control block include CCKPLS and DWNSTR, while the communication-control block's inputs include RDRAM, WRRAM, PLSCK, and RDPLS.

Physically, the DRAM-control state machine **(Fig 3a)** is a free-running, 3-bit Johnson counter. It continually generates six timing states for each read, write, and refresh DRAM cycle. At the end of each timing cycle, the DRAM read/write state machine **(Fig 3c)** changes state and remains constant for the duration of the next timing cycle. The DRAM-control state machine then drives the DRAM-control signals' logic to generate the actual DRAM-control output signals. The signals generated for each of the six timing states depend on the cycle type specified by the DRAM read/write state machine. The DRAM-control state machine's ENDCY output signals the end of each cycle.

A problem crops up

Referring to the DRAM read/write state-transition diagram **(Fig 2b)**, you would expect the DRAM to be continually receiving refresh cycles when no access requests are coming in and the system is idle. However, by observing the RAS− and CAS− signals at the DRAM ICs with your logic analyzer, you see that the DRAMs are oscillating between refresh and read cycles. This symptom is your first indication of an error. However, determining the exact source of the problem is difficult because there are two states that will generate read cycles—namely, the Read and Pre-Read states. These states are indistinguishable on external LCA pins.

In traditional TTL or PLD debugging, you would be able to examine your design's subcircuits with your logic analyzer or oscilloscope, observing more of the details of the error. However, with the LCA, these nodes are buried deep inside.

Now the route-out method comes into play. First

FPGAs rewrite the rules

The field-programmable gate array (FPGA) features faster turnaround and lower risk than a mask-programmed gate array. FPGAs, plus the proper design tools, help streamline time-consuming and costly design cycles. One kind of FPGA is the Xilinx logic-cell array (LCA). LCAs combine traits of both PLDs and gate arrays. As with PLDs, you can program them yourself, eliminating the nonrecurring engineering costs and lead times associated with gate arrays. Like gate arrays, LCAs have a flexible, nondedicated architecture.

Programming defines the LCA's internal logic and I/O configuration. Additionally, LCAs have more registers than PLDs, making them much more efficient for register-intensive designs. With gate counts as high as 9000, an LCA's level of integration is like that of a medium-sized gate array.

On-chip RAM, rather than permanently blown fuse links, determines LCAs' configuration. Hence, you can reprogram them as often as you like—both during the development cycle and once they are in the field. Because you can correct LCA design errors faster and more inexpensively than gate arrays', RAM-based LCAs don't need costly, time-consuming suites of exhaustive test vectors.

The LCA has a rectangular array of configurable-logic blocks (CLBs), which contain both storage and combinatorial-logic elements. The number of CLBs depends on the size of the LCA. Currently, the number ranges from 64 to 320.

A ring of I/O blocks (IOBs) containing I/O buffering and storage elements surrounds the CLBs. Even the smallest LCAs have 58 I/O blocks. A grid of bus lines and programmable transistor switches interconnect the CLBs and IOBs.

The first choice for route out is an LCA pin not used in your design and not connected to other circuitry in your system.

you must decide which signals you want to route out. In this case, you decide to route out the two DRAM read/write state-machine bits, because they determine the DRAM cycle, and are your best way to identify the error source. Specifically, these are the DMOD0 and DMOD1 signals shown in the schematic (**Fig** 3).

Entering the LCA editor, you can determine the DRAM-control circuit's location. **Fig 4a** shows the 11 CLBs used for the DRAM-controller circuitry. In general, the signals associated with the DRAM-control circuit will be in this area, but you need to pinpoint their locations so that you can decide how to reroute them.

Use the Hilight command to locate the nets' current routing. **Fig 4b** shows both DMOD0 and DMOD1. According to the first criterion for selecting a route-out pin, clearly the nets are closest to the right-hand edge of the LCA package, and therefore pins along that edge are more desirable.

In this particular design, all of the right-hand pins connect to external circuitry, so you must select pins that can temporarily be route-out pins. Considering the second criterion for selecting a route-out pin, you see that most of the routing channels near the right-edge pins are already used. However, keep in mind that when temporarily using a pin from your original

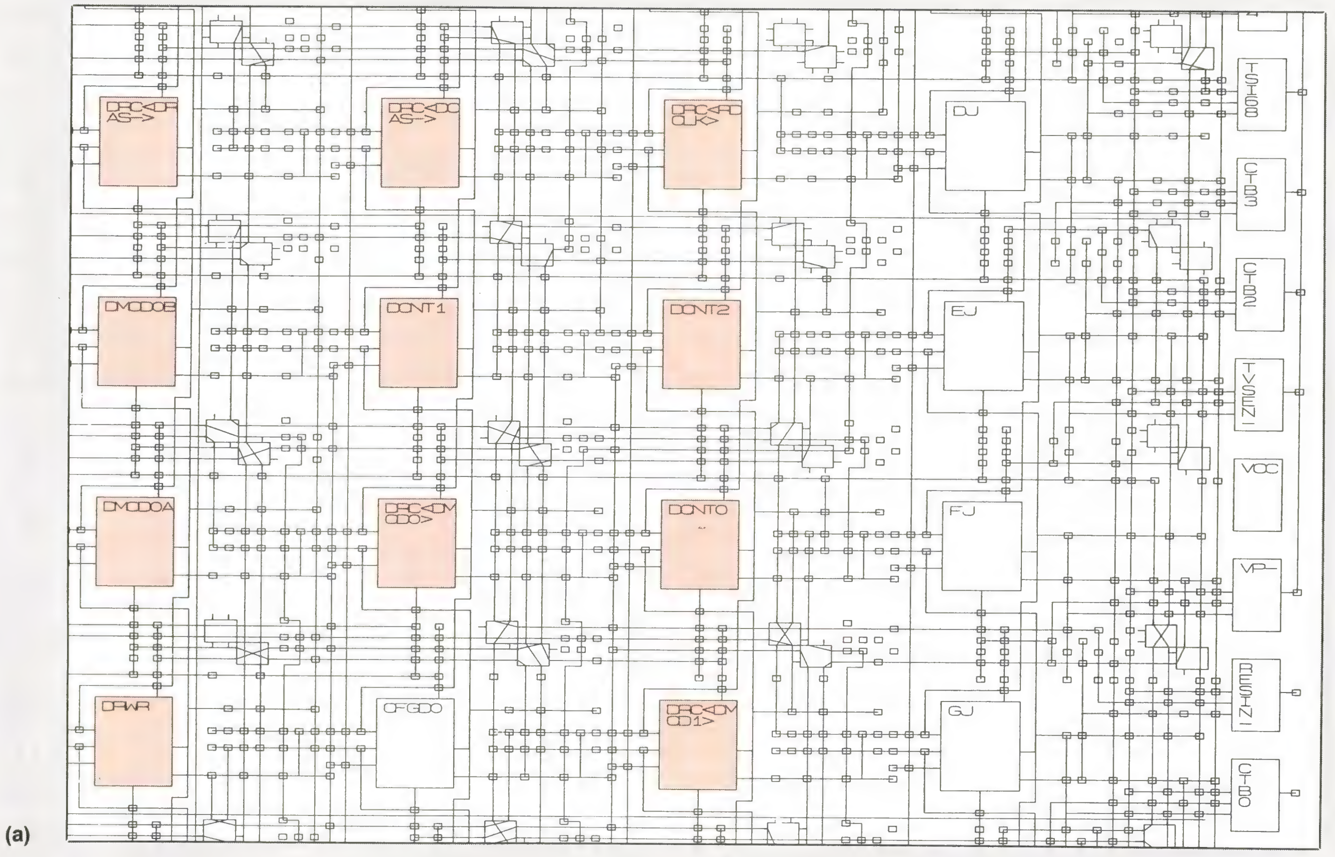
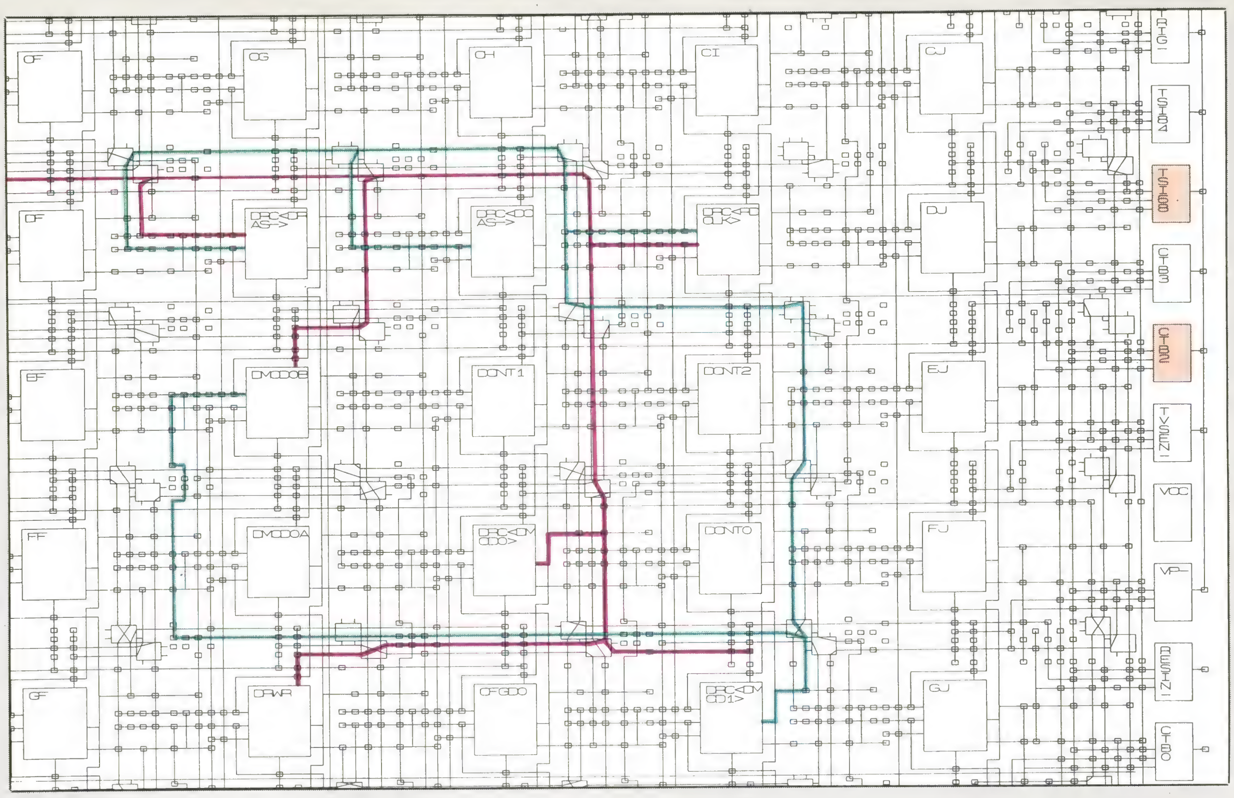
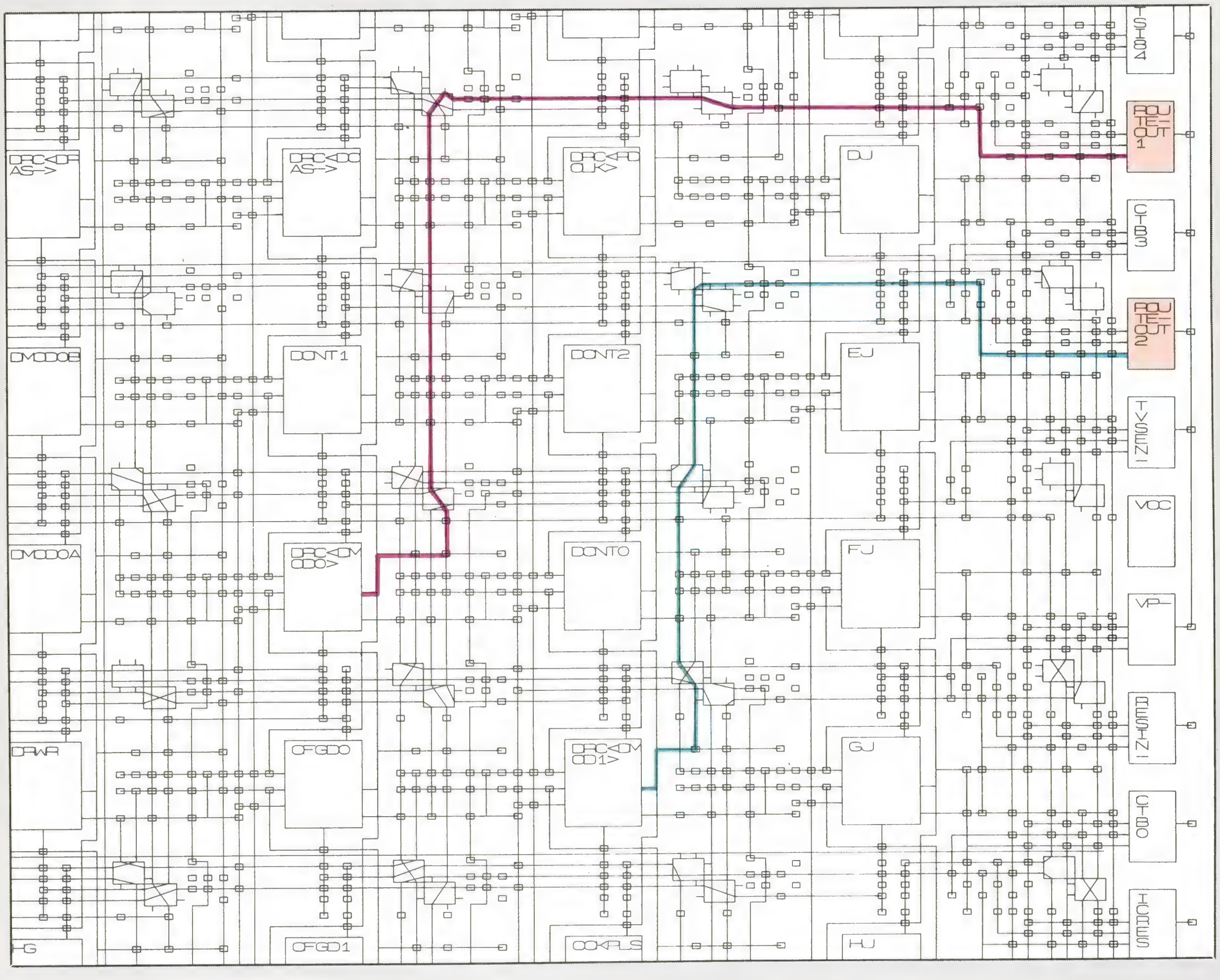


***Fig 4—This LCA implementation of the schematic** in **Fig 3** shows **a**, the highlighted CLBs, which compose the DRAM-control block; **b**, the highlighted nets and IOBs selected for route out; and **c**, the nets and pins after completing the route out.*


CF
CG
CH
CI
CJ
DF
DRC<DR AS->
DRC<DC AS->
DRC<RD CLK>
DJ
EF
DMCDOB
CONT1
CONT2
EJ
FF
DMCDOA
DRC<DM CDO>
CONTO
FJ
GF
DRWR
CFGDO
DRC<DM CD1>
GJ
VCC
VP-

(b)


DRC<DR AS->
DRC<DC AS->
DRC<RD CLK>
DJ
ROU TE-OUT 1
DMCDOB
CONT1
CONT2
EJ
ROU TE-OUT 2
DMCDOA
DRC<DM CDO>
CONTO
FJ
VCC
VP-
DRWR
CFGDO
DRC<DM CD1>
GJ
CFGD1
CCKPLS
HJ

(c)

Like gate arrays, LCAs have a flexible, nondedicated architecture.

design for route out, the routing channels previously used for the pin will be available for route out, too.

The CTB2 and TSI68 pins provide the best fit to these criteria; **Fig 4b** shows their locations. Comparing their locations to the highlighted nets and the available routing channels, you find that the DMOD0 net will route most easily to TSI68 and the DMOD1 net to CTB2.

You have now selected route-out pins (IOBs) by considering their routability. The next step is to configure the IOBs for route out. Use the editor's DelBlk command to delete the previous configuration, their original names, and the existing routing from the TSI68 and CTB2 IOBs. Now is a good time to rename these pins with the NameBlk command, either with their old names or new names that indicate that they are route-out pins (in this example, TSI68 becomes ROUTE-OUT1 and CTB2 becomes ROUTE-OUT2). Now use the EditBlk command to edit one of the IOBs and configure it to be an output with the configuration command BUF:ON (2000 series). Use the EndBlk command to finish editing the block.

Repeat this process for the other route-out IOB, or alternately, use the CopyBlk command to copy the first IOB's configuration into the second. Next, you use the AddPin command to connect the route-out pins to the highlighted nets.

Specifically, to execute the AddPin command, select the DMOD0 net as the source and the ROUTE-OUT1 IOB .o pin as the destination. This command makes the logical connection from the net to the pin. Repeat this step for the DMOD1 net and the ROUTE-OUT2 IOB .o pin. The final step is to route the new connections using the Route command, selecting the DMOD0 and DMOD1 nets. In this example, because of the forethought in selecting pins and the nature of the design, the LCA editor can automatically route both nets. **Fig 4c** shows that you now have the two internal DRAM read/write state machine bits routed out to external pins.

Now for the moment of truth. You download the routed-out design into your system and once again observe the DRAM oscillating between read and refresh cycles. However, this time you can also observe the DRAM read/write state machine bits directly, in real time, and discover the DMOD1 bit toggling on alternate cycles. From **Fig 2b** you can see that the read cycle occurs because of an erroneous transition to the Pre-Read state. With this new level of detail, you return to the schematic and are able to pinpoint the faulty logic.

You have now debugged the DRAM-controller circuit with the route-out method. Though this example has been a fairly simple case history of a faulty circuit, it does demonstrate the effectiveness of using the route-out technique to increase the observability of your LCA design during debugging. The ability to observe internal states helps decrease the time spent debugging because this observability provides more detail about the bug and reduces the amount of guesswork involved.

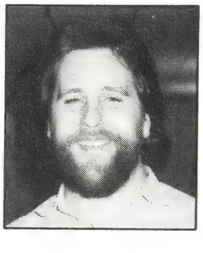
In-circuit verification

The major difficulty often encountered when trying to use the route-out method is the lack of pins available for route out. Most LCA designs utilize all pins in the design, leaving no free pins for route out. When the LCA is in circuit, the output pins are not always available for temporary use as route-out pins, because they are controlling the target system. We developed the route-out method while perfecting our Mesa I in-circuit verification tool, whose internal circuitry consists mostly of LCAs.

This instrument has a "shadow" LCA that operates in parallel with the target LCA in your prototype. The shadow LCA sees all the inputs from the prototype circuit that the target LCA does. Because the internal logic and the stimulus for both devices are the same, the two devices run in parallel. But the shadow LCA produces no outputs for the circuit under test.

Therefore, you can more easily use the route-out method in the shadow LCA when few or no pins are available for route out in the target LCA. The target-system LCA keeps the prototype operational, while the shadow LCA's outputs deliver vital internal information to your logic analyzer or oscilloscope. EDN

Author's biography



John Rostykus is a project engineer with Data I/O Corp (Redmond, WA), where he has worked for four years. Currently, he is a systems designer for in-circuit verification tools. John is a 1986 graduate of the California Institute of Technology (Pasadena, CA), from which he received a BSEE. In his spare time, he enjoys hiking, camping, and playing soccer.

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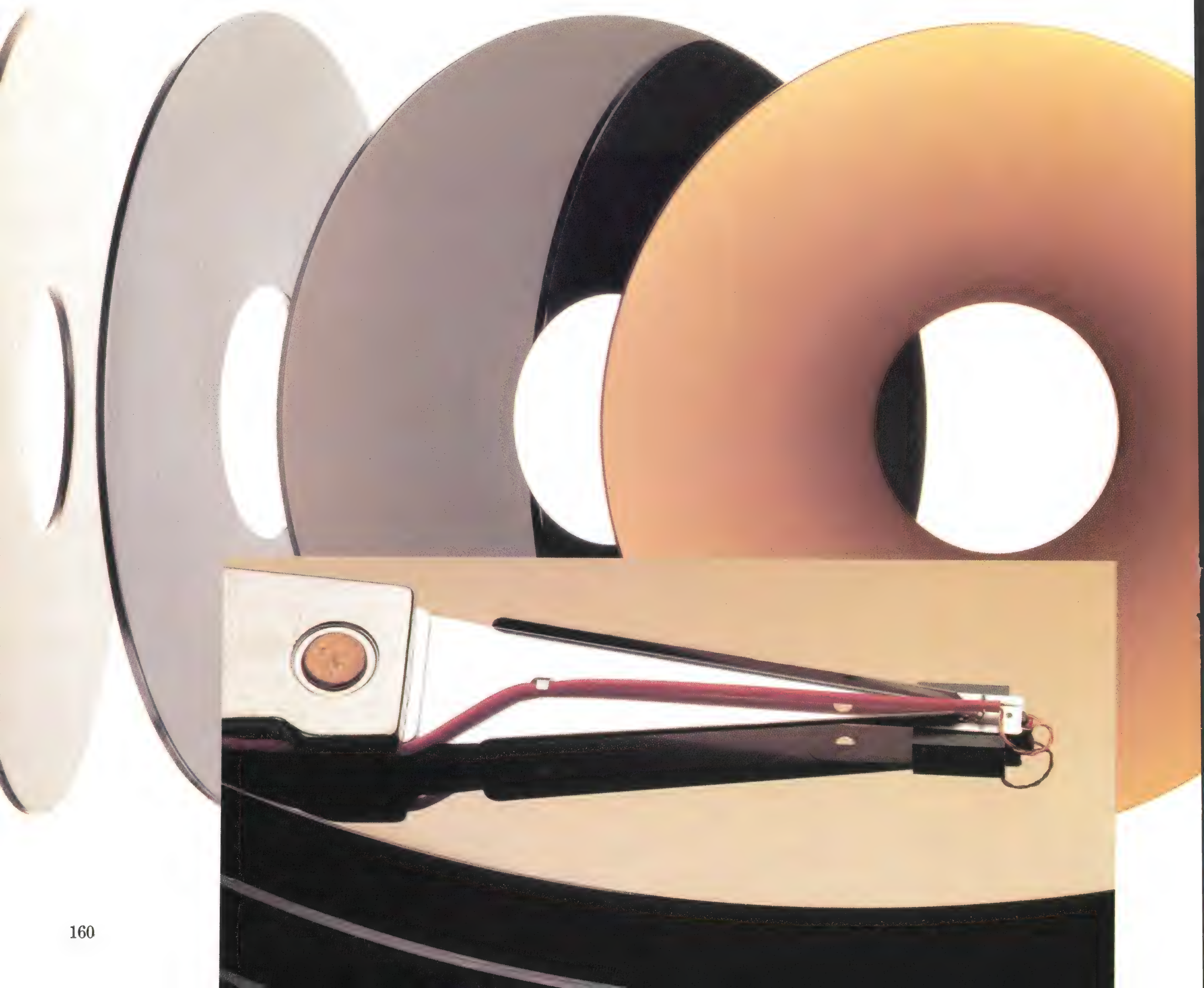

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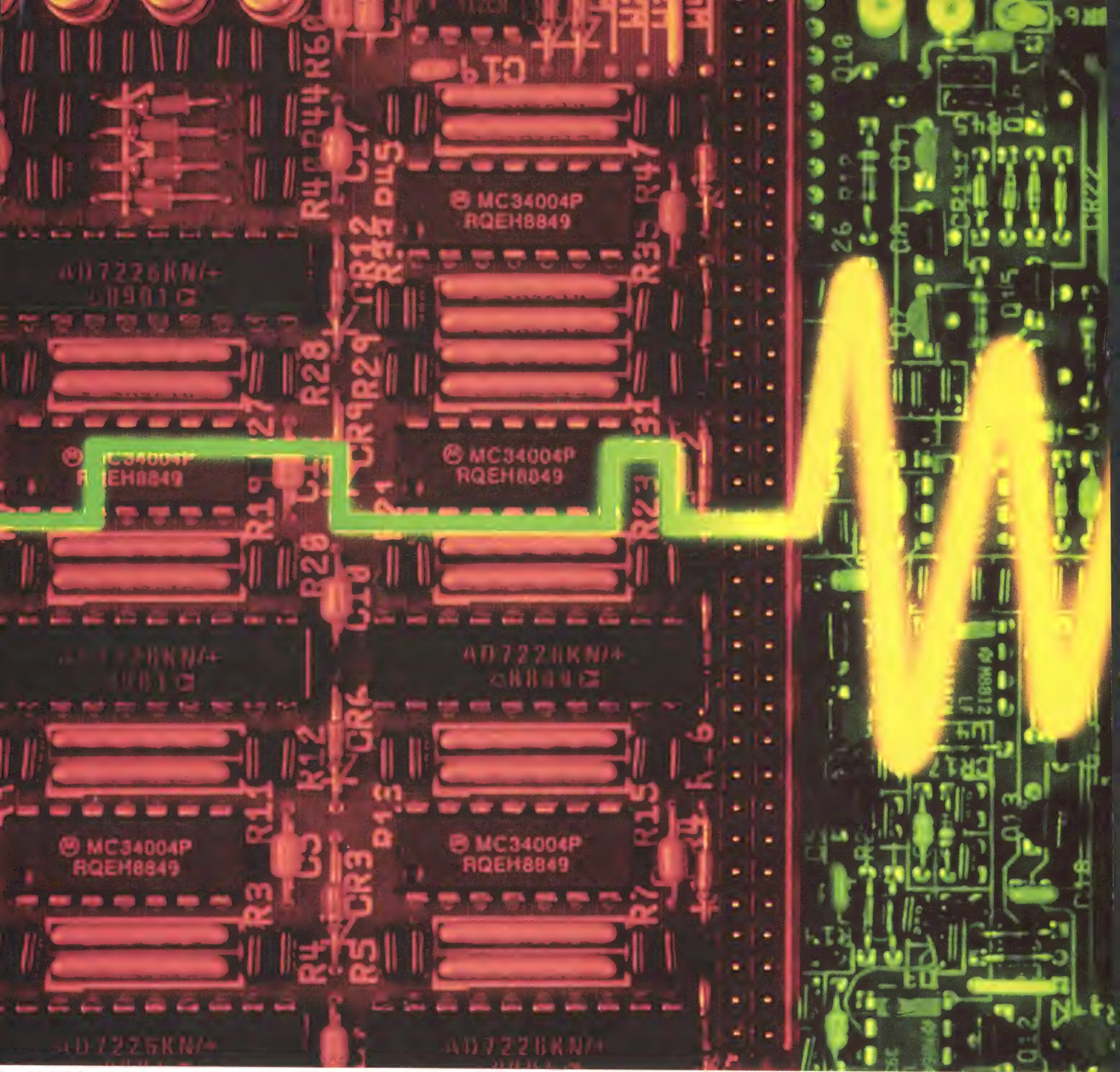

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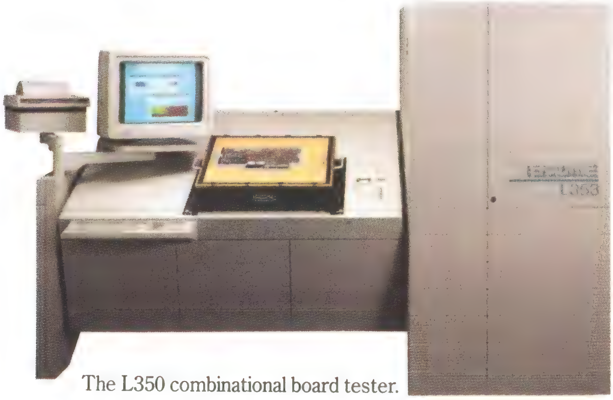

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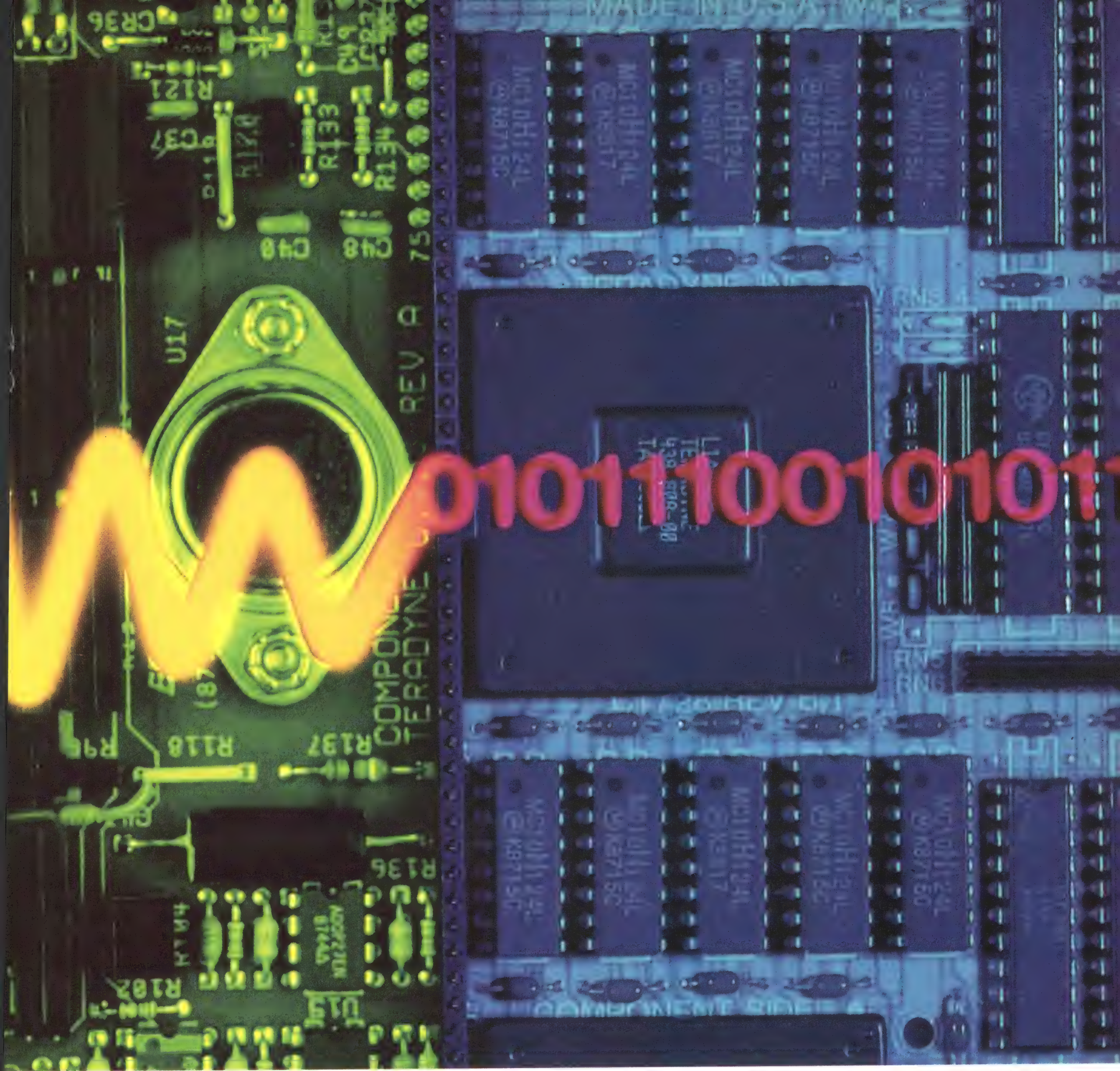

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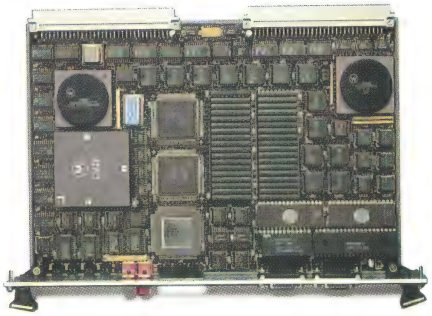

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CIRCLE NO. 78

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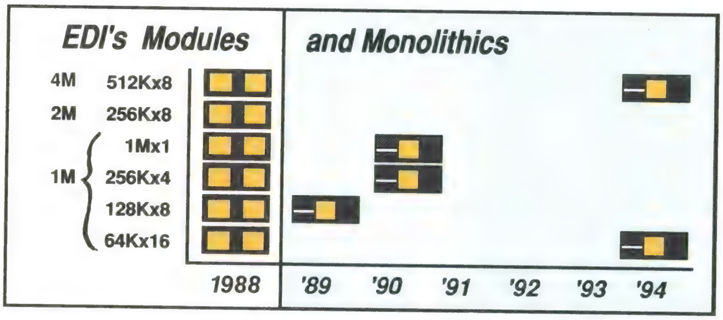

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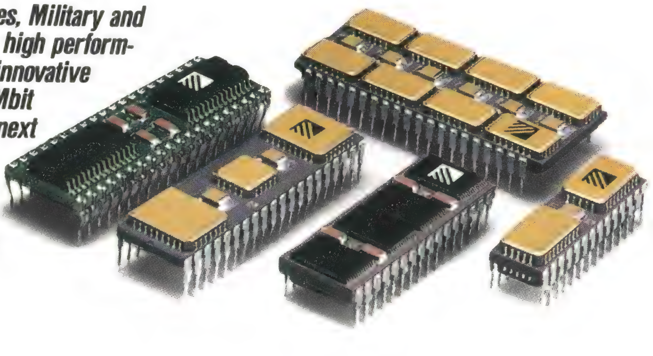

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CIRCLE NO. 79

Create accurate analog models for better simulations

Even the best simulator provides bad results if you use poor models. Although most commercial analog simulators come with libraries of device models, these libraries often lack the complex models you need. As a result, you may have to build your own models.

Eric S Filseth, Jeff Berwick, and Harold Mann,
Valid Logic Systems

An analog simulator can only simulate to the accuracy and detail of the models you use. The model libraries bundled with your simulator can't possibly contain all the device models you'll ever need, so you may have to build a model yourself. It's difficult to build an accurate and complete model of a complex analog device, because the model must emulate hundreds of possible device behaviors. However, if you have a graphic CAE system with modeling tools, a thorough working knowledge of the building blocks in the simulator, and a solid helping of creativity, you can build complete complex-device models.

The best way to construct such models is as black boxes. As long as the correct input results in the correct output, the actual construction of the model is irrelevant. Try to model functions as small circuits that recreate the desired behaviors but don't affect the other functions in the model.

The most important tools you'll need are a simulator and model library that support many basic functions. The library's functions should include different types of controlled sources, ideal switches, and mathematical function blocks such as differential equations. These basic building blocks are very useful in creating analog-simulation models.

In addition, you must have a manufacturer's specification of the part you intend to model. Then, you'll need to define which of the hundreds of circuit behaviors are most important to your application. Also, you'll want the models to simulate quickly while providing coarse but accurate emulation, so you'll usually use behavioral descriptions to model complex devices. Finally, the creation of accurate and complete analog-device models demands more creativity and expertise than digital-device modeling does.

The optimization problem

In creating component models for simulation, the main difficulty is making sure the model simultaneously gets all the behaviors right. The characteristics of a semiconductor component are functions of a set of manufacturing rules: any given rule, such as n^+ doping density, is likely to impact many otherwise unrelated electrical characteristics. Building a model is like trying to solve Rubik's Cube; trying to develop the model without knowing the manufacturer's rules is like trying to solve the cube blindfolded. Further, in developing a model from the schematic, you'll probably find that a tweak to improve one parameter adversely affects other parameters.

To build accurate and complete models, the most important tools you'll need are your ingenuity and your knowledge of the behaviors you're trying to model.

The problem with building complex models, therefore, is how to optimize a set of linked nonlinear characteristics simultaneously. In fact, this simultaneous optimization is the only effective way to extract simulation parameters for discrete devices such as transistors. Engineers have developed elaborate computer techniques for this purpose.

Complex analog devices are potentially even more difficult to model. If functions are interdependent, tweaking one function will force you to tweak all the others as well. If your approach isn't systematic, you could spend the rest of your life tweaking parameters and still not derive the data necessary to drive the model.

For system simulations, you'll build most models at the macro level. Building a macromodel is a straightforward task. First, determine which behaviors you need to model. Then, develop circuit-level models for each behavior. Finally, integrate the behavior models into a single macromodel.

Emulate the right behaviors

The biggest disadvantage to this approach is that a macromodel is an approximation that emulates only those behaviors for which it was designed. On the other hand, building the macromodel one behavior at a time avoids parameter contention, and for integrated circuits with many active devices, this coarse system-level macromodel usually simulates much more quickly.

In general, the linear response of an analog system is the easiest characteristic to model. You can describe the linear responses concisely by using a set of mathematical equations. Typical examples are the gain and phase response of an amplifier and the relationship between torque and power in an electric motor. You could use some combination of function blocks and linear elements such as resistors and capacitors to model these relationships.

The op amp is a common linear component in analog design. The Boyle **(Ref 1)** and Hu **(Ref 2)** models are the most common op-amp behavioral models. The transient response is a good vehicle for separating and modeling linear and nonlinear behaviors. The principal linear behavior is frequency response. The following equation models the frequency response:

$$\frac{V_{OUT}}{V_{IN}}=H_0\frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)\cdots}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\cdots} \quad (1)$$

where p_1 and p_2, z_1 and z_2 are the respective frequencies of the poles and zeros; s is the frequency of the stimulus; and H_0 is the dc gain. This equation models behaviors such as whether the amplifier will oscillate at low gains and how long it will take to settle to a final value. The model is accurate within the component's linear operating region; outside of the linear region, the slew rate and other factors come into play.

One important nonlinear characteristic for most op amps is the device's slew rate. The slew rate is essentially the maximum value of dV_{OUT}/dt that the circuit topology can support. The internal circuitry of the op amp, which drives the compensation capacitor, limits the rate of change of an amplifier's output. At high frequencies, the current available to charge and discharge the capacitance is exhausted, and slew-rate limiting occurs.

The linear frequency response of the amplifier (**Eq 1**) defines a maximum bandwidth for arbitrarily small input signals. In many applications, however, the usable bandwidth of the op amp is limited to a much lower frequency than the linear model predicts. Distortion limits large-signal response when the input exceeds the maximum slew rate. And, at a given frequency, a large input signal demands a greater rate of change within the op amp than a signal of lower amplitude, indicating that even in the absence of clipping, the amplitude of the signal affects an amplifier's output. A macromodel provides a quick, accurate way to model the large-signal nonlinearity caused by slew-rate limiting.

For example, consider a unity-gain amplifier producing a 10-MHz, 5V triangle wave. Because of the 100-

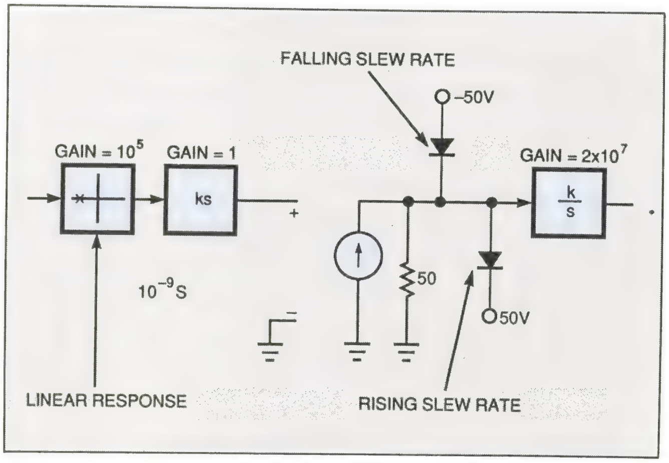


Fig 1—Often, the best way to build an accurate model *is to assign separate parameters to each condition you're trying to emulate.*

nsec period, the output must go from 0 to 5V in 50 nsec or 100V/µsec. If the amplifier had a slew rate of only 50V/µsec, then the output waveform would be distorted. The amplifier would be operating outside the linear region, and the equation would no longer be valid.

Had the signal been of smaller amplitude—for example, a 1V, 10-MHz triangle wave—**Eq 1** would still be valid. The output-voltage swing would be only 1V in 50 nsec, or 20V/µsec—well within the slew limit of 50V/µsec. This wave would pass unimpaired.

As long as the equation implies that dV_{OUT}/dt is less than or equal to the specified slew rate, the speed at which the amplifier's output can change is given by the equation; otherwise, the device's actual dV_{OUT}/dt is equal to the slew rate. Incidentally, this discrepancy is the reason why many manufacturers specify both large-signal and small-signal bandwidths on their op amps and similar components.

Real-world analog systems often process signals of continuously varying amplitudes and frequencies, and components pass in and out of their linear ranges often and quickly. An accurate simulation requires a model that accounts for both large- and small-signal behaviors.

The problem with modeling these systems is that the same physical components affect both the slew rate and the op amp's linear response. These components include the device physics of the transistors, the bias current selected by the manufacturer, and the parasitic capacitance (C_c). If you chose to use the chip's actual schematic for the model, you'd have to find values for these attributes that would simultaneously produce results for the rising slew rate, the falling slew rate, and the linear response.

Fig 1 presents an easier way to model analog behaviors. Though it bears little resemblance to the actual chip, this circuit lets you separate the linear and the two nonlinear responses (rising and falling slew rates may be different) and independently assign parameters to them. A single-pole gain block models the linear response. A differentiator block differentiates the linear output voltage, and the two diode-and-battery clamps—along with the current source and resistor—determine the specific range of the derivative dV/dt. Finally, a 1/s function block re-integrates this voltage (you could also use a current source and capacitor).

The two diode clamps limit dV/dt, the rate of change of the output voltage. By limiting the derivative, you can independently assign the linear response and the rising and falling slew rates.

This description outlines the basic procedure for modeling analog behaviors. Unless you specifically design in characteristics of the actual device, those attributes won't appear in the model. For example, one property of an op amp's topology is pole splitting, in which increasing the compensation capacitance actually causes the second pole of the linear response to increase in frequency, further stabilizing the amplifier. The model in **Fig 1** doesn't include pole-splitting effects and may give poor predictions under certain circumstances, such as when you use uncompensated, high-bandwidth op amps in low-gain applications.

Fig 2 is a more complete model that does exhibit pole splitting; it uses the structure from **Fig 1** and implements a few additional behaviors. For example, a single resistor implements open-loop output impedance and a single source models input offset voltage. Notice that both of these behaviors are isolated; changing their value doesn't affect the rest of the model.

To simulate these analog systems, you can use a popular analog-circuit simulator such as Spice. In addition, you can add some digital logic to your mostly analog systems and still simulate with Spice. Adding the digital logic, however, requires some modeling support: logic-gate and switch-level building blocks are essential. From these simple models, you can build more complex models.

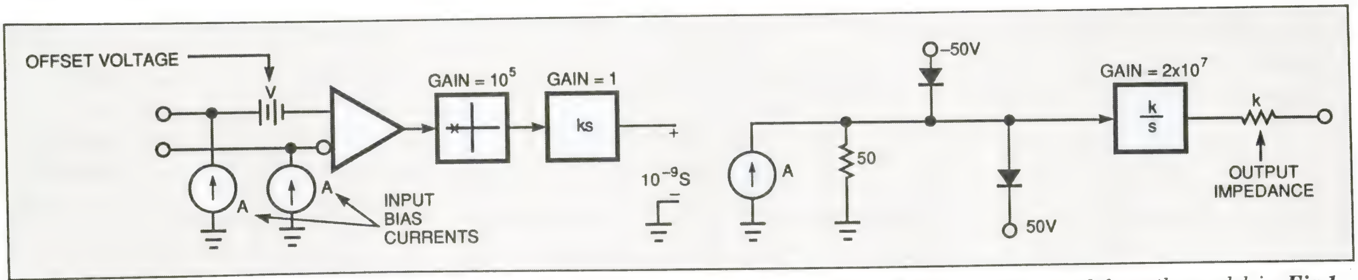


Fig 2—In many cases, the model looks nothing like the component that it's mimicking. *This model, derived from the model in* ***Fig 1****, also accounts for open-loop output impedance and input offset voltage.*

Consider your models to be black boxes; as long as they mimic the external characteristics properly, the models' internal operation isn't important.

The circuit in **Fig 3**, for example, implements an analog-to-digital converter of variable precision. Once you've built this model, you can then use it as a building block, or "primitive," to emulate more complex systems.

This model is based more on a mathematical idea than on any particular circuit, although it's similar to a successive-approximation converter. The model is built from 1-bit converter cells. You can increase the precision by daisy chaining more stages together.

The first step in building the model is developing a truth table that describes the behaviors you want to model. Consider, for example, a converter cell in which the digital output, B, indicates whether the input, A, exceeds the reference, V_{REF}. The analog output, C, is the signal that the converter passes to the next cell in the chain.

Fig 3 implements the behavior from **Table 1**. The comparator, IC$_1$, provides the digital output behavior, which determines whether the input signal is greater than or less than the reference voltage and supplies the appropriate signal at point B. The analog output behavior at C is slightly more complicated; it depends on the digital output. Input signal A drives the current source/resistor combination. If the digital output is high, then the circuit subtracts the reference signal, V_{REF}, from reference A; otherwise, the circuit subtracts ground. S$_1$ chooses between V_{REF} and ground. If you were daisy chaining the models together, you'd then reference the next cell—or succeeding bit—in the chain to $V_{REF}/2$.

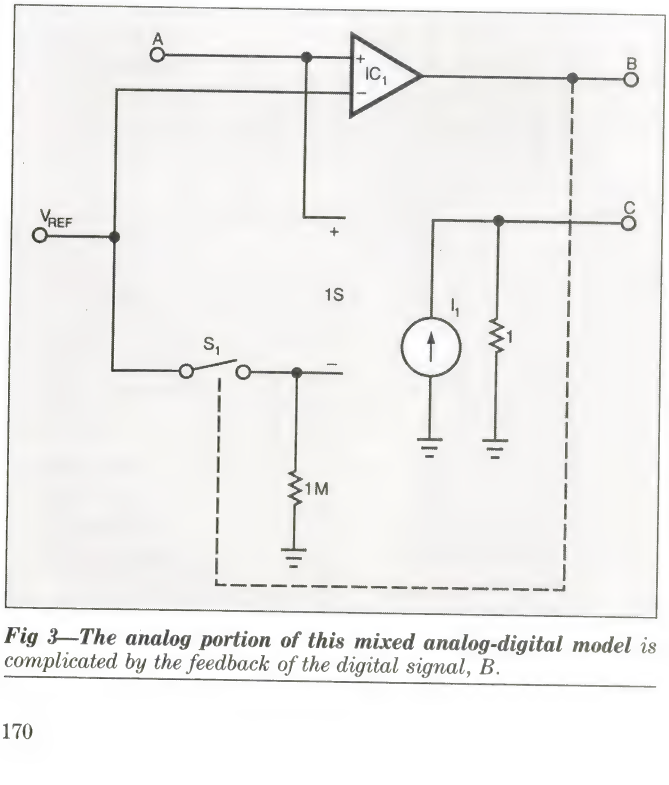


Fig 3—The analog portion of this mixed analog-digital model *is complicated by the feedback of the digital signal, B.*

Table 1—Converter-behavior model

Condition	B	C
A ≥ VREF	1	A − VREF
A < VREF	0	A

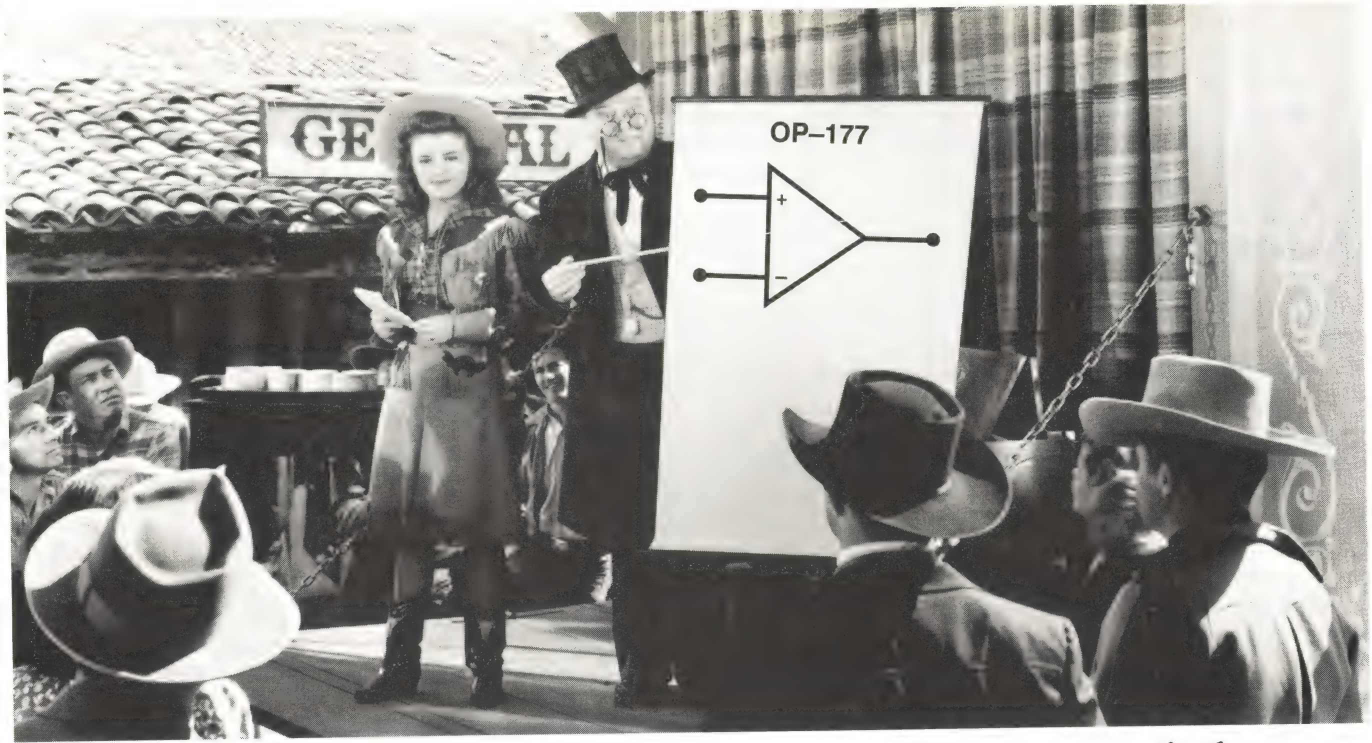
You can use Spice and its derivatives for the simulation of more than just electronic circuits. Spice is a common tool for solving sets of simultaneous differential equations. One example is the modeling of heat flow, for which you can build models easily.

Consider the silicon transient suppressor. This device is a type of zener diode that limits voltage or current impulses in a connection and converts the electrical energy to heat, thereby protecting more sensitive circuitry from damage. This device is useful for examining sophisticated analog macromodeling.

General Semiconductor Industries (GSI) manufactures a line of transient suppressors under the trademark name "TransZorb" that have high thermal capacity and low series resistance. The 1.5KE Series can handle 1-msec impulse-wave transients as high as 1500W. Consider a model from GSI's 1.5KE line that can simulate transient suppression for accurate analyses of protective circuitry. For this analysis, the model should have certain features: the model's breakdown voltage should change with junction temperature; the junction temperature of the model should be a function of time and input power; the junction capacitance should be a function of reverse voltage; and the forward junction voltage should be a function of temperature. Finally, you should be able to use the same macromodel for the entire family of devices.

The model should simulate a suppressor's V-I characteristics and the dynamic thermal effects, which increase the clamping voltage, ultimately limiting the effectiveness of a transient protection scheme. For descriptive purposes, you can break the model into two sections. An electrical model describes the V-I characteristics of the device, and a thermal model calculates the power dissipation and describes the thermal characteristics of the silicon and its surrounding package.

In **Fig 4**, which combines a thermal model from **Ref** 3 and an electrical model from the device's databook, components R$_3$, V$_5$, and D$_1$ describe the reverse-break-



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CIRCLE NO. 80

Analog components operate in both their linear and nonlinear regions, so build your models to emulate both small- and large-signal behaviors.

down characteristics of the suppressor. These components allow the device to shunt current from A to B when voltage V_a is exceeded. Resistance r_b is a function of the breakdown voltage and plays an important role in determining the clamping effectiveness of the device. The simulator calculates this resistance when you enter V_a as a component value using the empirical relationship

$$r_b=(2\times10^{-4})\ (V_a^2). \qquad (2)$$

Diode D_2 serves a dual purpose by simulating the junction capacitance and the forward-bias characteristics of the unidirectional suppressor. R_4 models the forward series resistance of the device, and R_5 simulates leakage.

You could use the electrical model alone to simulate the suppression of low-energy, short-duration pulses. For higher-energy pulses, the model must take into account the positive TC of the breakdown voltage.

The thermal model simulates a temperature rise by employing the electrical analogues for heat (current) and temperature (voltage), a method which both **Refs 3 and 4** describe in detail.

A voltage-controlled current source (VCCS), I_1, senses the instantaneous input voltage applied to the device; VCCS I_2 tracks the current through the suppressor using R_3 as a sense resistor. Multiplier F_1 calculates power dissipation ($P=V\times I$), and VCCS I_3 translates the result to a current so that 1A corresponds to 1W.

The network of resistors R_7 through R_9 and capacitors C_1 through C_3, which you should choose to match the time-domain thermal response of the 1.5KE Series suppressors (JEDEC numbers 1N6267 through 1N6303), represent the thermal resistance and thermal mass of the TransZorb. In the model in **Fig 4**, heat flows through the thermal impedance to a final baseline temperature, represented by battery V_3. The baseline voltage, amb, relates to the user-specified ambient temperature, t_a, using

$$\text{amb}=t_a-27, \qquad (3)$$

where 27 represents the Spice-analysis default temperature of 27°C.

Battery V_1 translates the baseline temperature to its Celsius value, allowing you to read the instantaneous junction temperature directly as an output voltage on probe C (1V=1°C). To complete the thermal model, the voltage source V_4 translates the temperature rise at the point T to an incremental increase in breakdown voltage through the scale factor TC. When you enter the breakdown voltage (V_a) into the model, the simula-

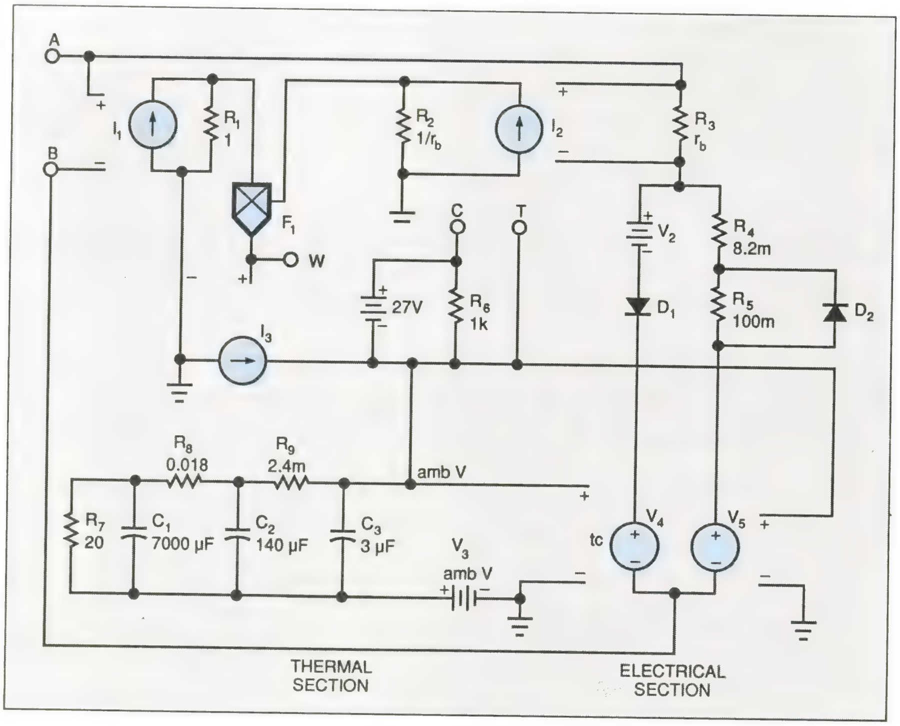

Fig 4—You can use simulation models to emulate thermal effects *in addition to modeling voltage and current characteristics.*

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CIRCLE NO. 81

You can build thermal models using electrical analogues for the heat and temperature of the component.

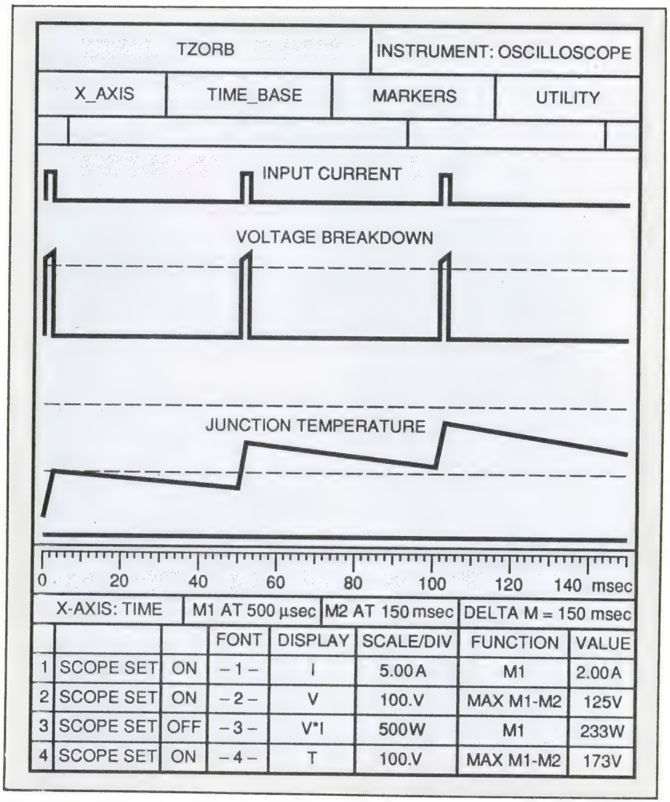
tor uses the model to calculate TC like the series resistance. According to the manufacturer's data, the empirical relationship for TC is

$$TC=(3.08\times10^{-4})\ (V_a^{1.145}). \qquad (4)$$

Source V_5 simulates the temperature coefficient of the diode's forward-voltage drop, using a typical value of −2 mV/°C.

The resulting model allows you to observe the clamping action, the effectiveness of the TransZorb diode at high temperatures and current, the simulated junction temperature, and the instantaneous input power. By entering the parameter V_a in the model in **Fig 4**, you select the device type for a low-voltage, unidirectional clamping suppressor in the 1.5KE Series (Models 1.5KE6.8 through 1.5KE100).

Fig 5 shows the simulation of a transient overload condition and illustrates the performance of a unidirectional model. When the simulator applies 1-msec, 2A spikes to a 110V suppressor, the device's voltage (middle trace) rises slightly beyond the specified breakdown voltage because of series resistance. During the suppression of the transient, the junction temperature (bottom trace) increases quickly. You can confirm the junction temperature's rise using the readout pin, which indicates that the device remains within a safe thermal operating range during the analysis. One interesting effect shown in the model is that the absolute breakdown voltage changes as the temperature increases. **Fig 5** illustrates this effect as a positive slope in the V-breakdown waveform during the three applications of power. The simulation evaluates how much transient energy this protection scheme can absorb before damage occurs to either the circuitry in parallel with the suppressor or to the protective device itself.



X-AXIS: TIME	M1 AT 500 µsec	M2 AT 150 msec	DELTA M = 150 msec

			FONT	DISPLAY	SCALE/DIV	FUNCTION	VALUE
1	SCOPE SET	ON	– 1 –	I	5.00 A	M1	2.00 A
2	SCOPE SET	ON	– 2 –	V	100.V	MAX M1-M2	125V
3	SCOPE SET	OFF	– 3 –	V*I	500W	M1	233W
4	SCOPE SET	ON	– 4 –	T	100.V	MAX M1-M2	173V

***Fig 5—In this simulated response to a series of current spikes,** the junction temperature droops with time, simulating heat dissipation.*

Watch out for these model failures

The consequences of using inadequate models in simulation range from minor glitches that require further analysis to expensive manufacturing failures. Inaccurate models come in two types. The first type simply doesn't emulate the behavior that will destroy your circuit. For instance, a model that doesn't include temperature variance won't represent how the device will operate outside a narrow range of operating conditions. This type of omission is insidious; the model may perform perfectly in simulation, even though the actual device fails in operation.

In the second type of inaccurate model, the model provides a wrong answer in simulation, either because of erroneous data or because the model was constructed erroneously. This type of model inaccuracy is sometimes easier to spot. If you find problems of this sort, you'll have to go back and re-examine the construction of your black box.

The key to avoiding these problems is to know beforehand which behaviors you need to model. Also, keep in mind that even though the mathematical model itself is "perfect," the chips you use vary from unit to unit, and this component variance can seriously impact factory yields. To save yourself time and trouble and ensure that your model always works, simulate worst-case as well as best-case scenarios. EDN

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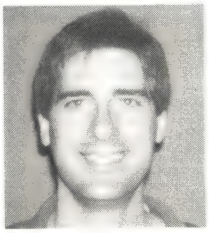
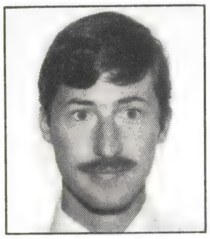
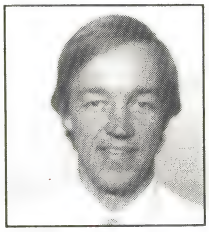
Authors' biographies



Eric Filseth is a product marketing manager for analog-design tools at Valid Logic Systems. He earned a BSEE from Stanford and an MBA from UCLA. Before moving into marketing, Eric was an analog-design engineer for a semiconductor vendor.



Jeff Berwick earned his BSEE and MSEE at Rensselaer Polytechnic Institute and is currently a senior applications engineer at Valid Logic Systems. His responsibilities include developing, describing, and testing applications for the simulation of analog-device models.



Harold Mann is a senior applications engineer at Valid Logic Systems, where he develops functional models and manages analog-library development. Harold has a BSEE from the University of Illinois at Champaign-Urbana.

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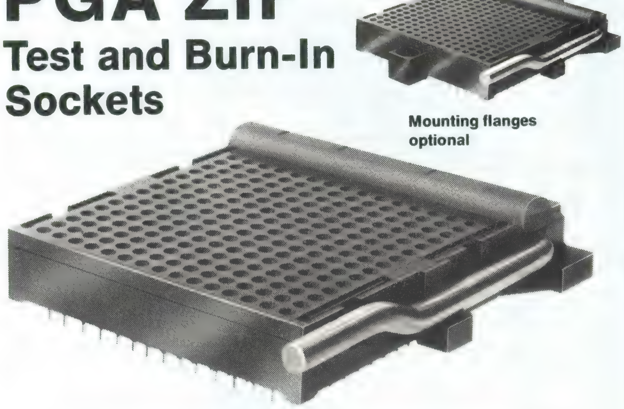

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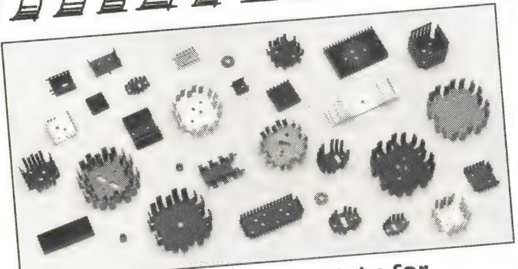

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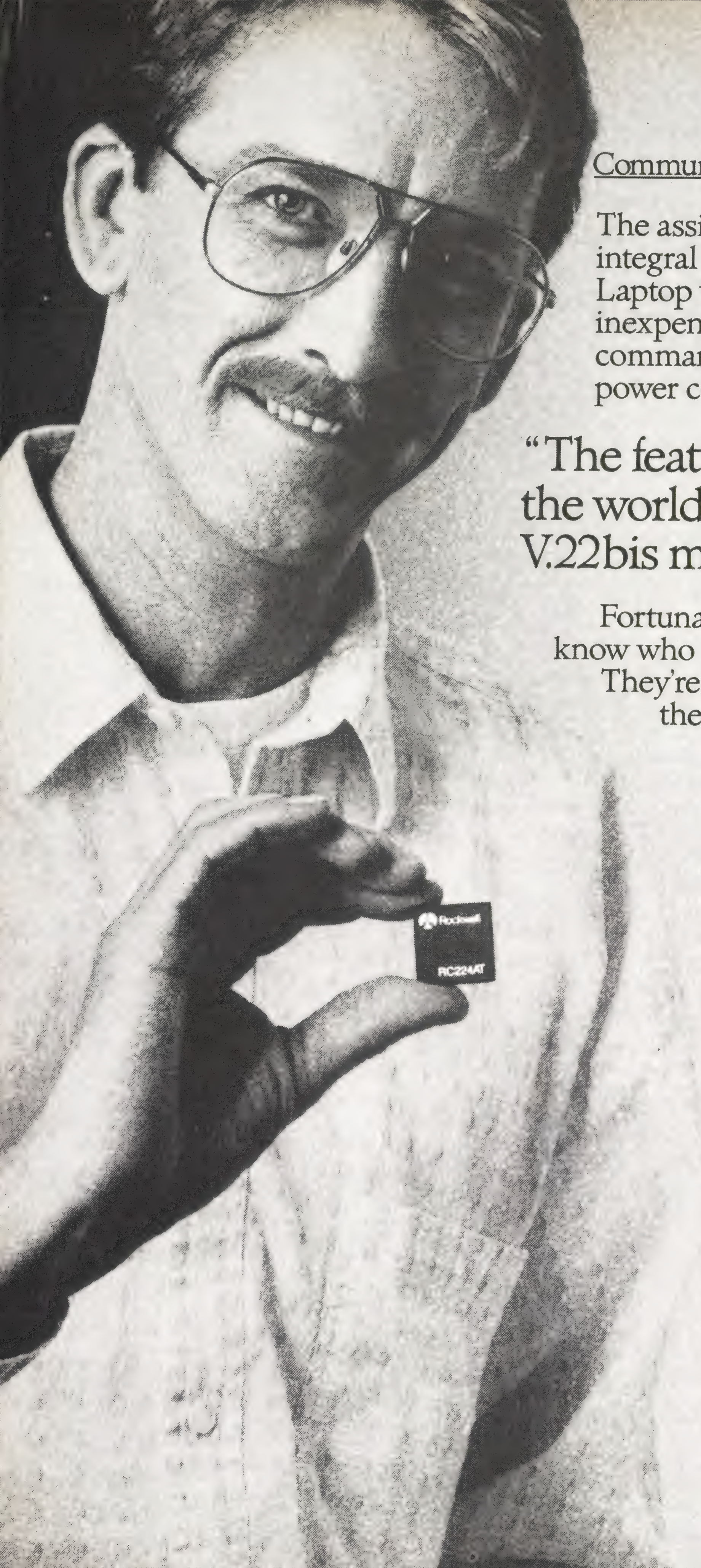

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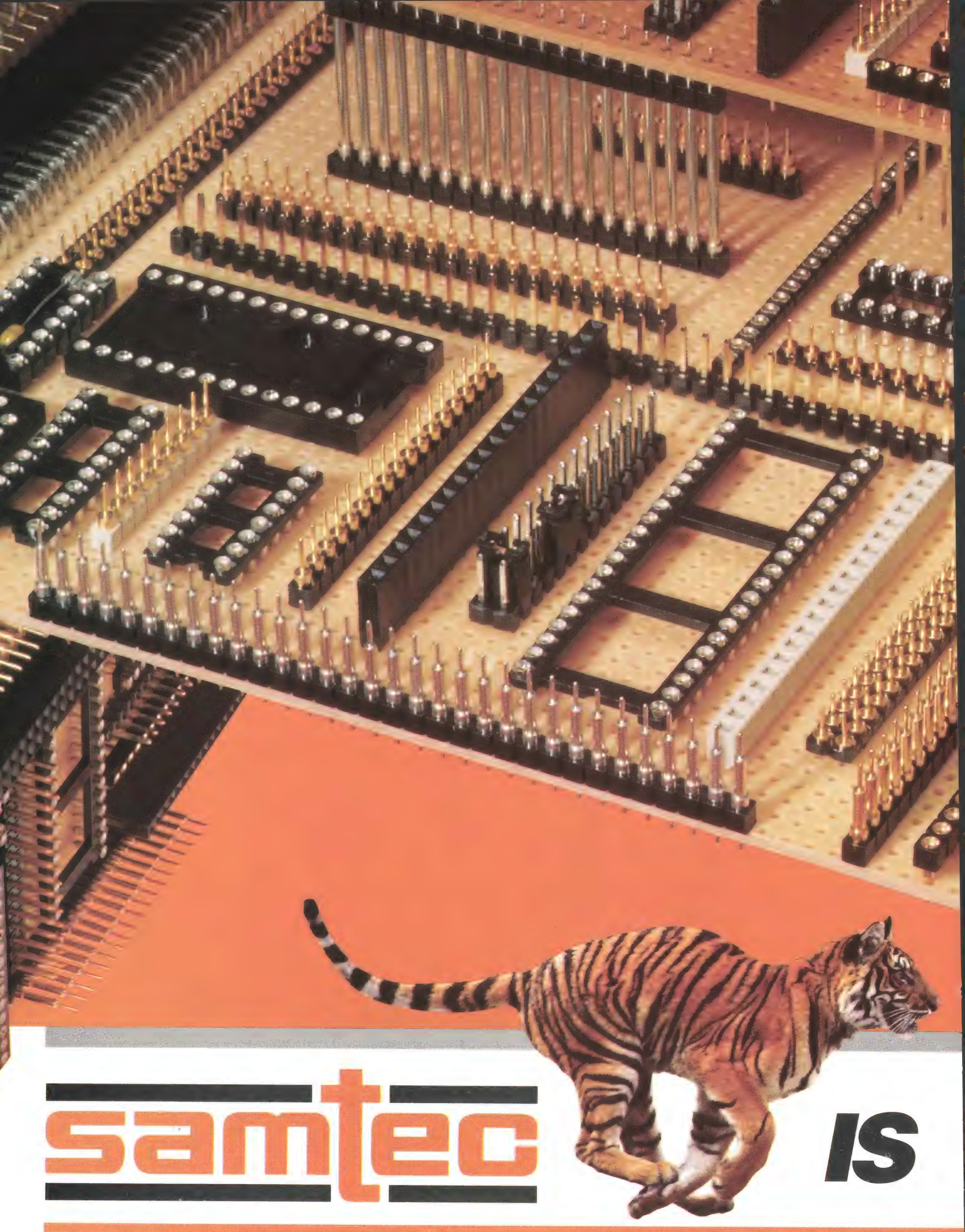

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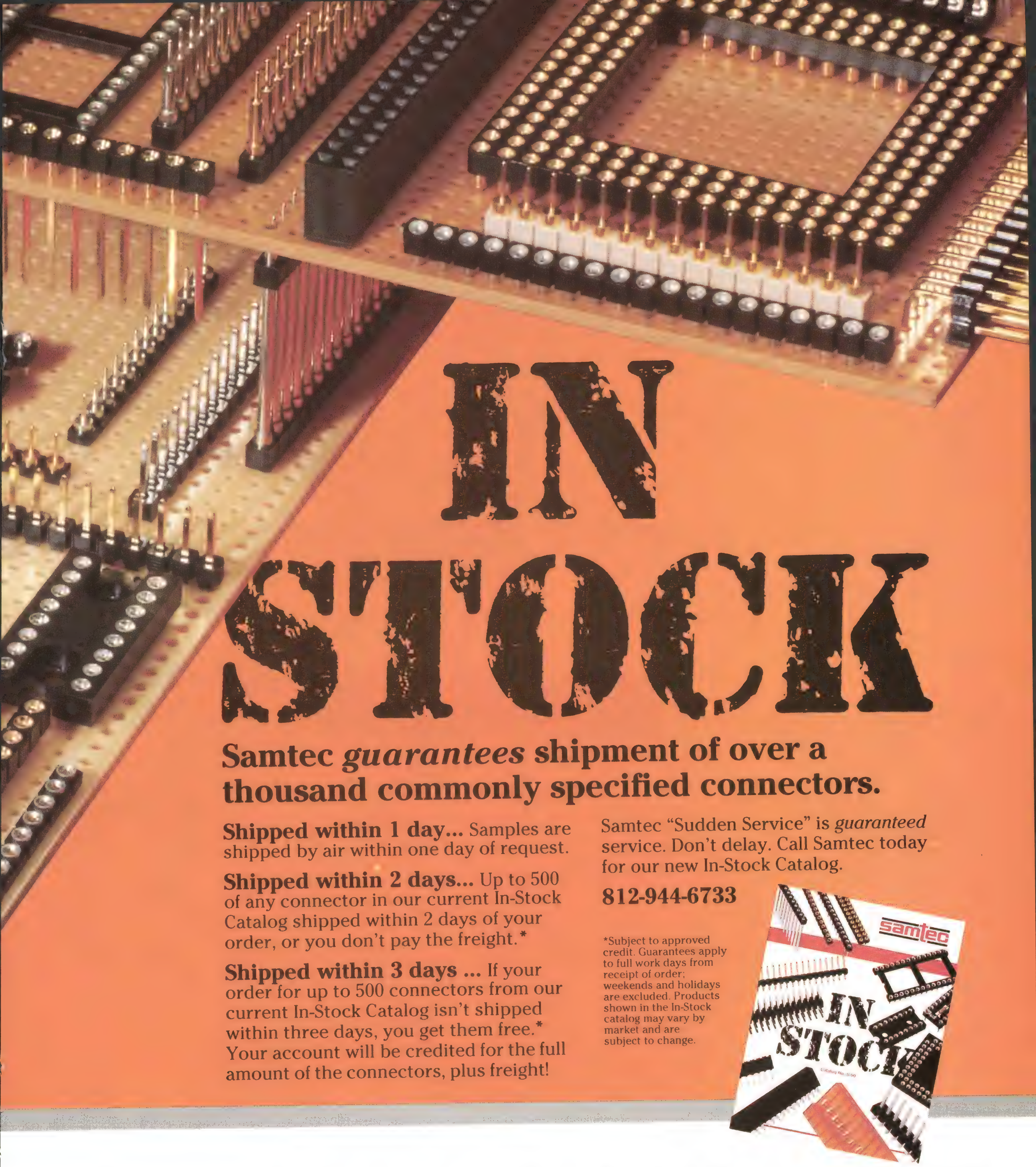

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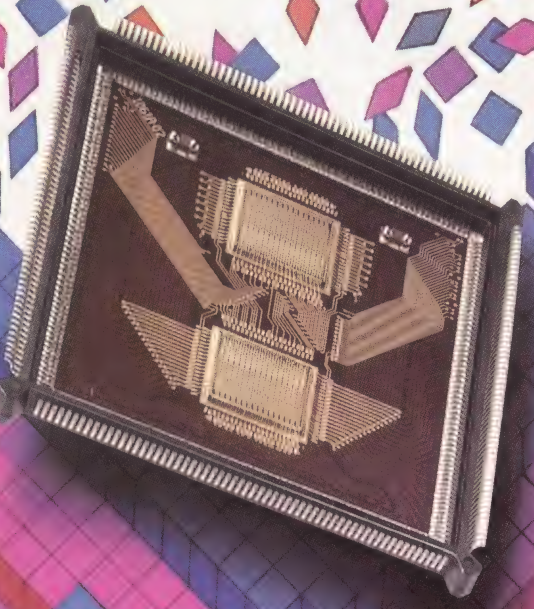

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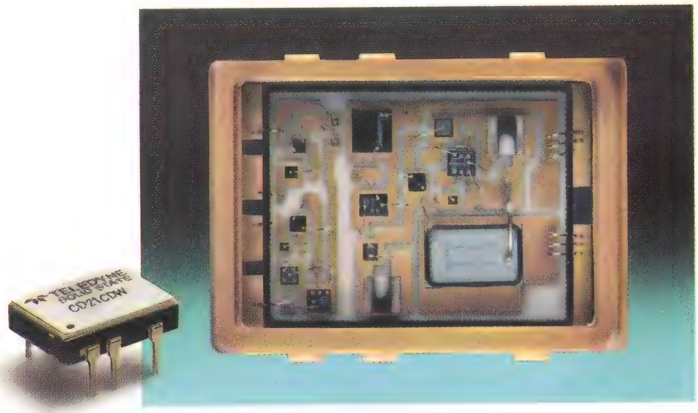

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Bias Current (I_{BIAS})		15.0	mA	$V_{BIAS} = 5 V_{DC}$
Control Voltage (V_{IN})	0	18.0	V_{DC}	
Control Current (I_{IN})		250	µA	$V_{IN} = 5 V_{DC}$
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Turn-On Voltage $V_{IN\,(ON)}$		0.3	V_{DC}	
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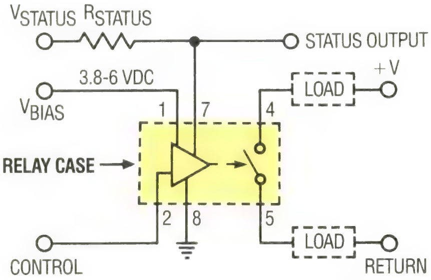
		0.7	A	+85°C
Output Trip Current (I_{TRIP})	2.4 (Typ.)		A	+25°C, 100ms
On-Resistance (R_{ON})		0.65	Ohms	
Turn-On Time (T_{ON})		1.5	ms	
Turn-Off Time (T_{OFF})		0.25	ms	
Status Voltage (V_{STATUS})	1	18	V_{DC}	
Status Current (I_{STATUS})		2	mA	$V_{SAT} \leq 0.3 V_{DC}$ See Note 2

Notes:
1. Series resistor is required for bias voltages above $6V_{DC}$. $RS = (V_{BIAS} - 6\,V_{DC})/15$ mA
2. A pull up resistor is required for the status output. $R_{STATUS} = (V_{STATUS} - 0.3)/I_{STATUS}$
3. Output will drive loads connected to either terminal (sink or source).
4. Status circuit is a built-in test feature checking the input circuitry of the relay. Status output is low (on) when the input is on.

All power FET relays may drive loads connected to either positive or negative referenced power supply lines (source or sink modes).



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CIRCLE NO. 86

High-voltage amp drives transducers

Don Michalski
University of Wisconsin Space Astronomy Lab, Madison, WI

The high-voltage amplifier in **Fig 1** provides 1500V at 2 mA to capacitive loads such as piezoelectric transducers. The amplifier's frequency response, however, is only a few hertz.

Photovoltaic isolators IC_2 and IC_3 bridge the low-voltage input section of the circuit and the high-voltage output FETs. The photovoltaic isolators produce an output voltage proportional to the current flowing through their input photodiodes. Operating the input photodiodes directly from the supply rails and in series with op amp IC_1's power pins minimizes crossover distortion.

Resistors R_5, R_6, R_8, and R_9 divide the high-voltage supply equally across the output FETs (750V max each). Because each FET has only a 1-kV rating, the circuit stacks several of them to achieve its 2-kV rating. Zener diodes D_3, D_4, D_5, and D_6 protect the FET's gates and do not normally conduct current.

R_7 and R_{11} determine the gain of the output stage's transconductance amplifier. The values of C_5 and R_{12} ensure stability for a 1-µF-max capacitive load. R_{13} and C_6 limit the input signal to a few hertz to prevent the unequal distribution of the high-voltage supply across the FETs at higher frequencies. EDN

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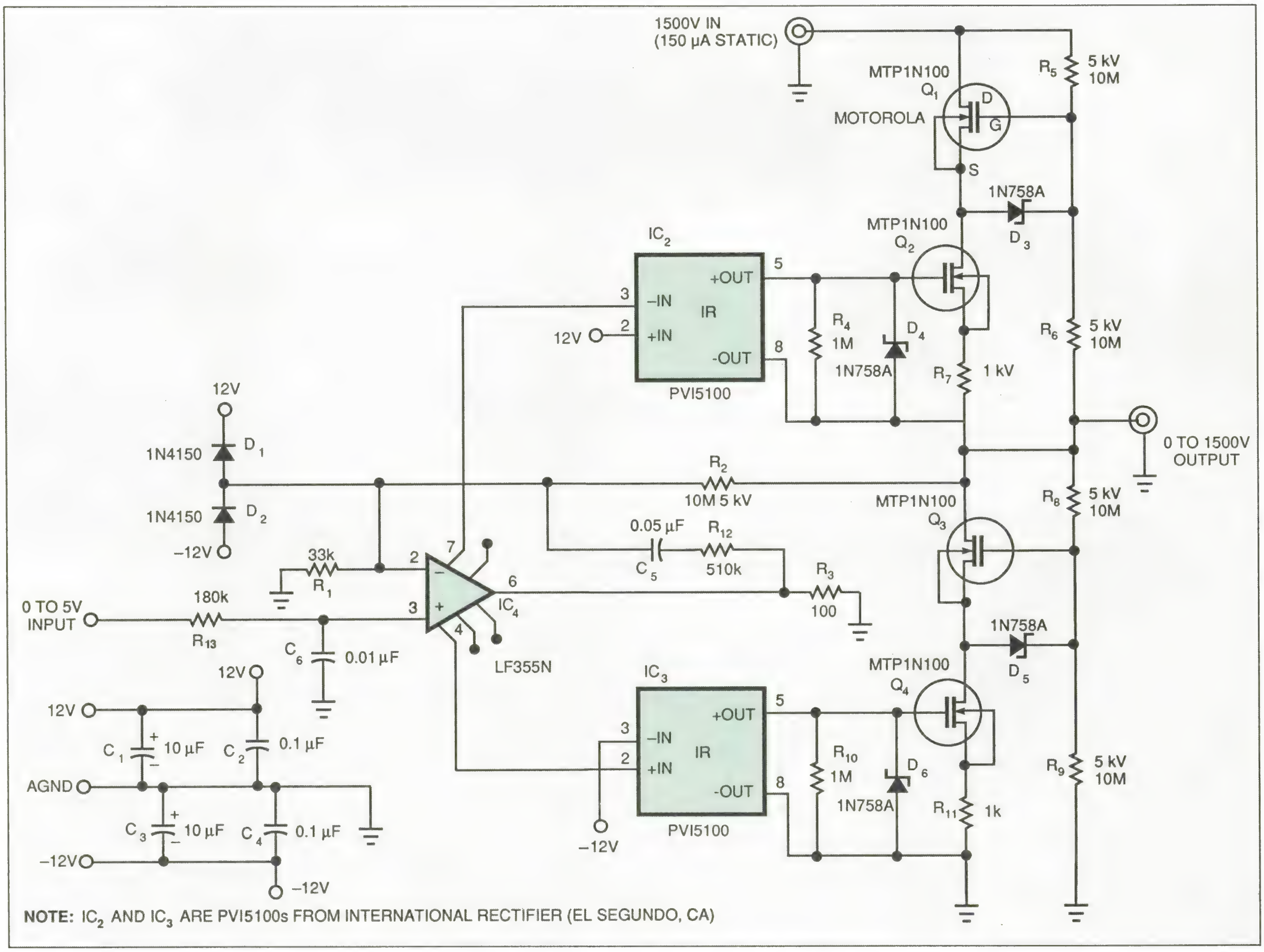


NOTE: IC_2 AND IC_3 ARE PVI5100s FROM INTERNATIONAL RECTIFIER (EL SEGUNDO, CA)

Fig 1—This high-voltage, low-frequency amplifier *can safely drive capacitive loads such as piezoelectric transducers.*

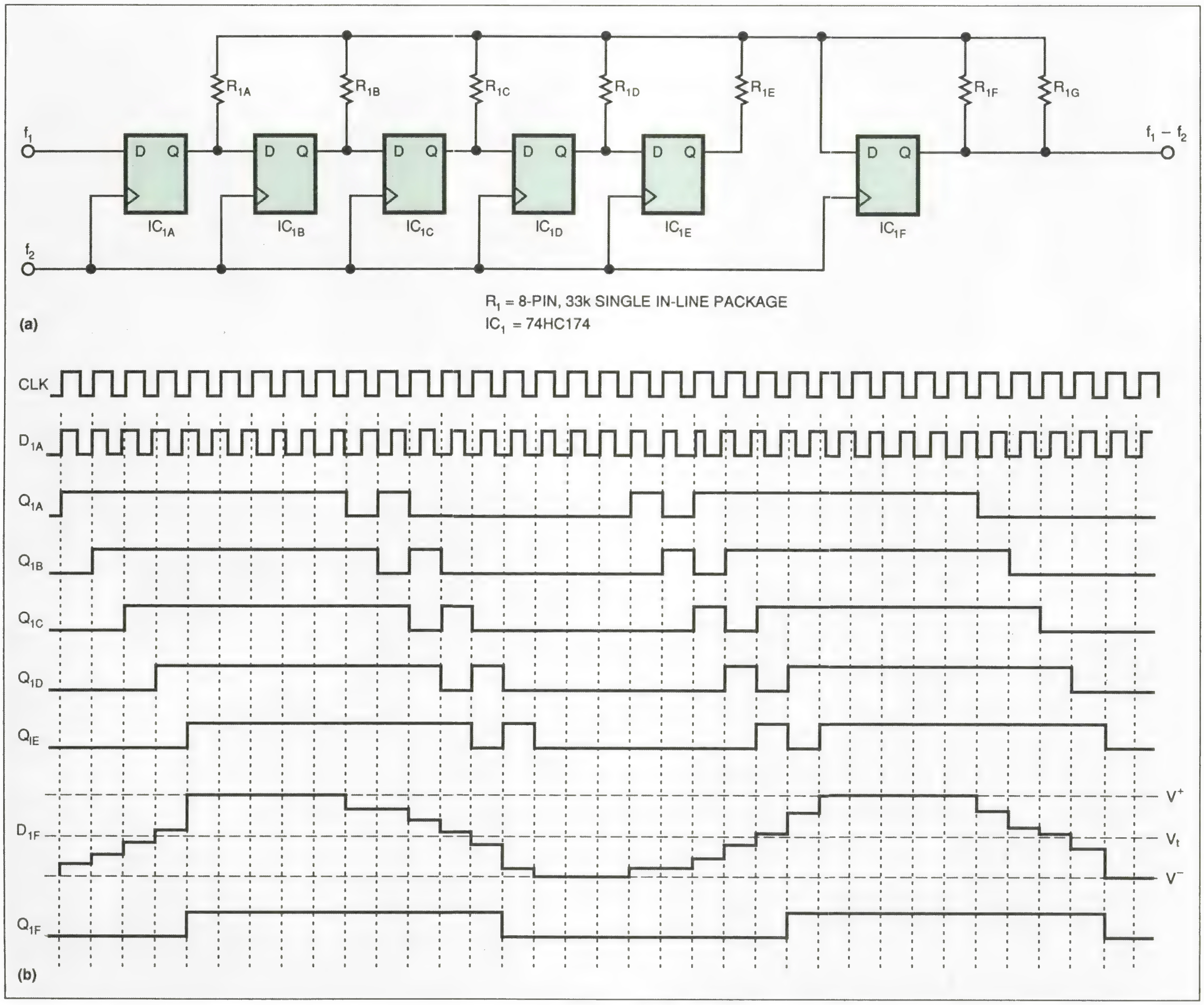
Resistor array debounces D flip-flop mixer

Milton Watts
Quartztronics, Salt Lake City, UT

The circuit in **Fig 1** overcomes the major limitation of mixers based on D flip-flops: output jitter arising from input phase noise. Simple D flip-flop mixers just apply the two frequencies to be mixed to the flip-flop's D and clock inputs. In the best of all possible worlds, the flip-flops's output would be the beat frequency between the two input frequencies.

In the real world, input phase noise can cause the output to toggle erratically when the two input frequencies are close together in frequency and phase. This circuit uses a chain of D flip-flops configured as a delay line to drive a resistor array in a single in-line package. The circuit's output does not change state unless the phase difference between the inputs persists for at least four clock cycles (**Fig 1b**). Therefore, the circuit is usually immune to jitter at the first flip-flop in the chain. **EDN**

To Vote For This Design, Circle No. 747



R_1 = 8-PIN, 33k SINGLE IN-LINE PACKAGE
IC_1 = 74HC174

Fig 1—The enhanced D flip-flop mixer in (a) *does not respond to changes at its input unless the changes persist long enough to traverse the D flip-flop delay line* ***(b)****.*

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MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

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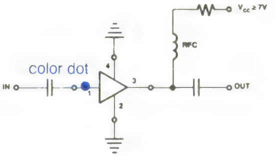

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CIRCLE NO. 87

Routine finds magic numbers

Russ Parker
Hewlett-Packard, Palo Alto, CA

The Turbo Basic program in **Listing 1** quickly finds the "magic numbers" for an integer fraction that closely approximates a given decimal. An example is the fraction $^{333}/_{106}$, which is only 0.00008 less than π. However, the program is set up to select two standard-value resistors for a voltage divider.

The key to the routine's speed is its presorted data. Study the subroutine "ldat," which generates a list of resistor values algorithmically. You should always use such an algorithmic technique for any component-value program rather than brute-force tables.

The program checks to see how closely the ratio of the numerator resistor and denominator resistor matches the desired output of the voltage divider. If the ratio is less than the target voltage, it increases the numerator; if the ratio is greater than the target voltage, it increases the denominator. When the ratio matches your accuracy limit, the program stops.

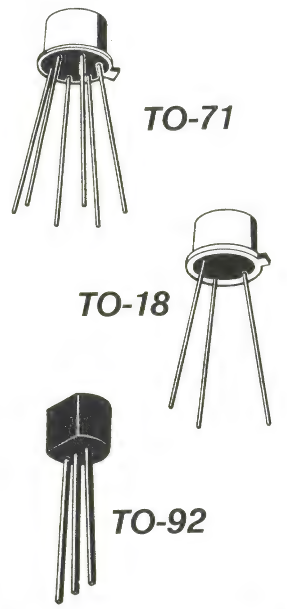
Send a self-addressed, stamped envelope for a program listing; send a self-addressed, stamped floppy disk for a copy of the program. The address is Russ Parker, c/o Hewlett-Packard, 3500 Deer Creek Rd, Palo Alto, CA 94303.

To Vote For This Design, Circle No. 748

Listing 1—Best-fit resistive voltage-divider program

```
    cls:screen 9
    color 12
    gosub ldat
strt:
    input "one supply voltage ",v1
    color 7
    input "other supply voltage ",v2
    color 10
    input "voltage desired ",v3
    color 14
    if v1>v2 then
        mosposv=v1:lesposv=v2
        else
        mosposv=v2:lesposv=v1
        end if
    if v3<lesposv or v3>mosposv then
         print "input error":delay 2:goto strt
    end if
    f=(v3-v2)/(v1-v2)      'calculate target number
    tend =1                'assign multiplier for 10x,100x resistors
    if f<.1 then tend=10
    if f<.01 then tend=100
    in=1:id=1:gosub getnew
lup1:

    if abs(newfrac-f) <delt then  'is new n/d better than best-so-far?
       delt=abs(newfrac-f)
       gid=d:gin=n            'store best-so-far numerator, denominator
    end if
    if newfrac> f then
         if id>res-1 then goto ste  'stop if there are no more values
       incr id                      'for denominator
       else
         if newfrac = f then goto ste   'stop on exact hit
         if in>res-1 then goto ste  'stop if there are no more values
         incr in                    'for numerator
```



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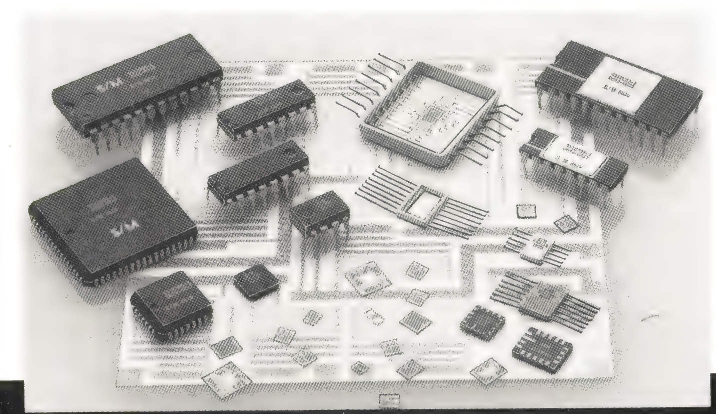

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CIRCLE NO. 89

Listing 1—Best-fit resistive voltage-divider program—*(continued)*

```
     end if
        gosub getnew                  '
     goto lupl

ste:
        print "resistors are ";
        print using "#.##";gin;
        print " and ";using "####.##";tend*gid
        print "Voltage generated, ";
        print using "##.###";(mosposv-lesposv)*gin/((gin+tend*gid))+lesposv
    end

ldat:
   'generate the table or resistor values
   'res=48      '2% table
   res=96       '1% table
   dim n(res)
   for I=1 to res
   resval=(10^(1/res))^(I-1)
   n(I)=.01*cint(100*resval)    'round values to actual manuf'd numbers
   next i
   return

getnew:
   n=n(in):d=n(id):newfrac=n/(n+tend*d)   'calculate scaled guess using
                                          'scaling multiplier
   if delt =0 then delt = 1-f
   return
```

8032 emulates itself

Tadeusz Jarosinski
FMiK ERA, Warszawa, Poland

The 8032 emulator in **Fig 1** takes commands from its host computer via Port A of the 8155 programmable interface adapter, IC_2. IC_{24} and IC_8 decode the host's reset signal to the 8032 to begin an emulation run. The emulator's debug monitor resides in the 2716 EPROM, IC_{19}. It uses IC_2's 256-byte internal RAM for temporary storage.

The debug monitor accepts commands to read and write to the 8032's internal data RAM and special-function registers as well as external program and data memories. The debug monitor uses the LCALL instruction to set software breakpoints in the emulator's 64k-byte max external memory (IC_{10} and IC_{17}).

Additional circuitry determines which memory space the 8032 will access when executing the debug monitor's MOVX @DPTR, A and MOVX A, DPTR instructions. Switches SW_1 and SW_2 let you emulate the WR and $\overline{RD}$ pins as bidirectional I/O ports P3.6 and P3.7.

Contact the author directly for information about obtaining a programmed 2716 or MS-DOS source files: Tadeusz Jarosinski, Design Engineer, FMiK ERA, Design Office, Liebniza 3, Warszawa, Poland, 01-481.

EDN

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Design Ideas continued on pg 192

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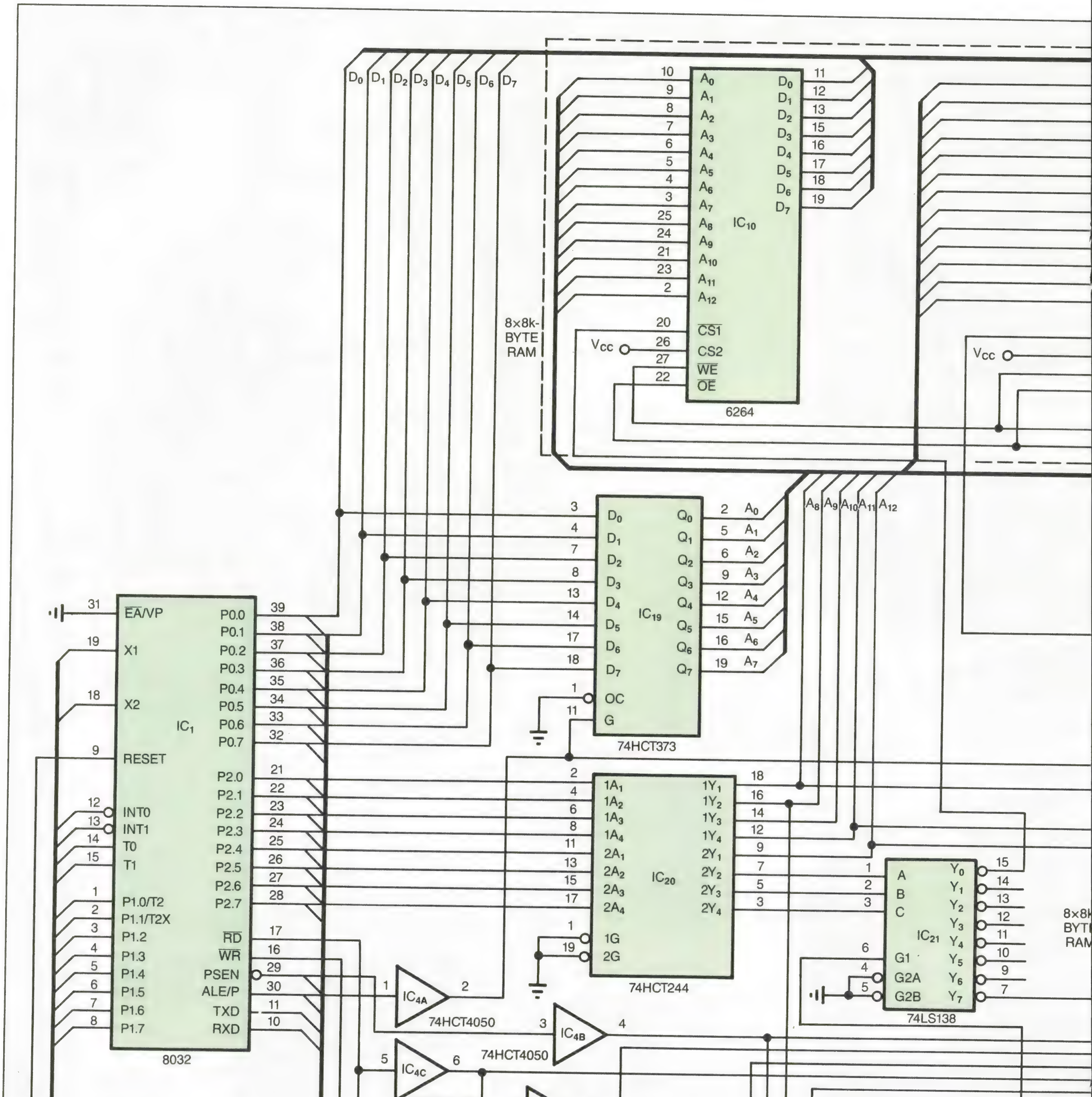
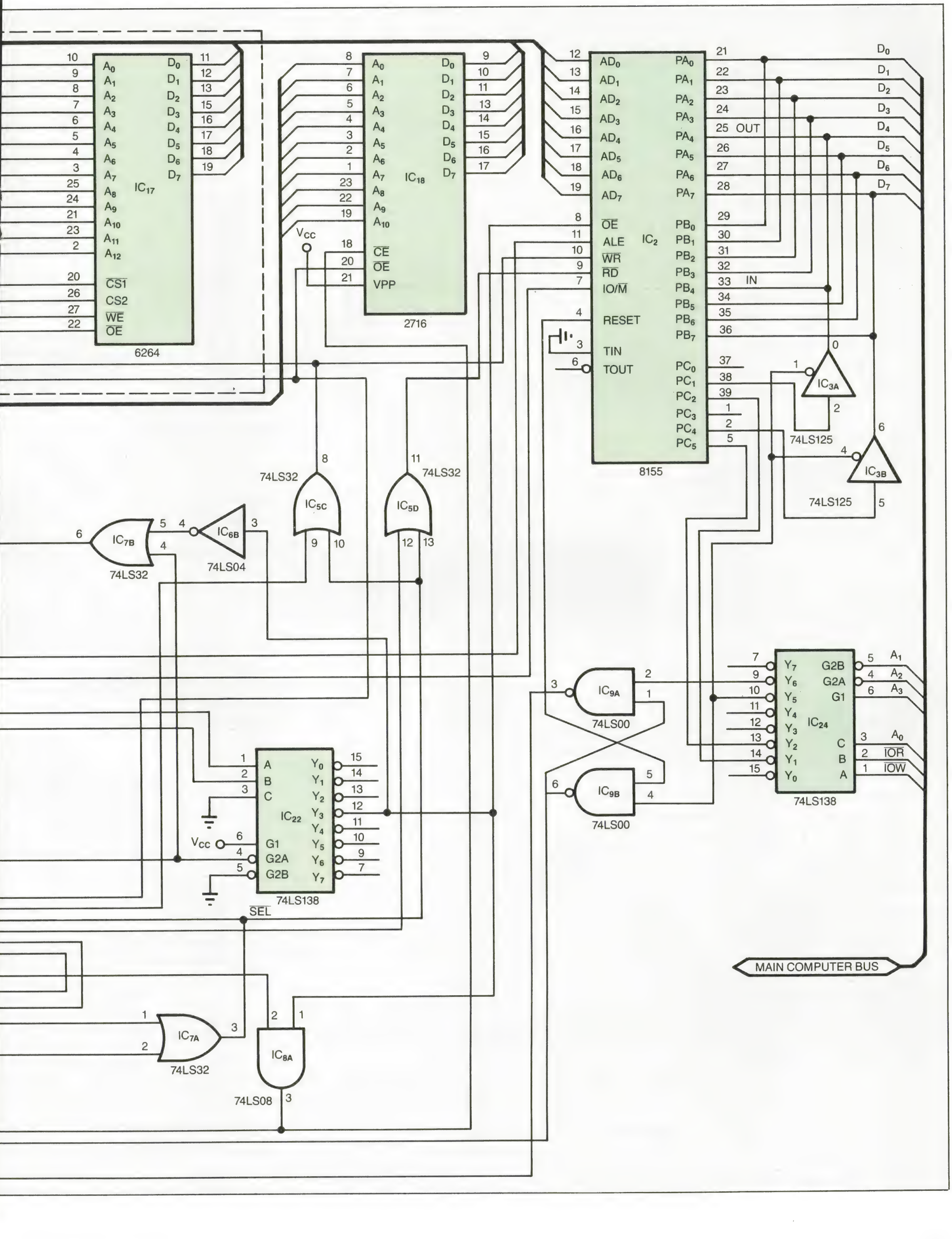


Fig 1—This 8032 emulator has a single-chip μP that connects directly to your target system.


IC17
6264
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
D0 D1 D2 D3 D4 D5 D6 D7
$\overline{CS1}$
CS2
$\overline{WE}$
$\overline{OE}$
IC18
2716
$\overline{CE}$
$\overline{OE}$
VPP
VCC
IC2
8155
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
$\overline{OE}$
ALE
$\overline{WR}$
$\overline{RD}$
IO/$\overline{M}$
RESET
TIN
TOUT
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7
PC0 PC1 PC2 PC3 PC4 PC5
OUT
IN
D0 D1 D2 D3 D4 D5 D6 D7
IC3A
74LS125
IC3B
74LS125
IC5C
74LS32
IC5D
74LS32
IC7B
74LS32
IC6B
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IC9A
74LS00
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74LS00
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A B C
G1 G2A G2B
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
VCC
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IC24
74LS138
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
G2B G2A G1
C B A
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IC7A
74LS32
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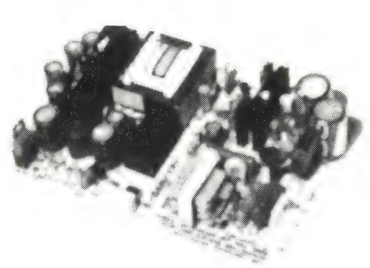

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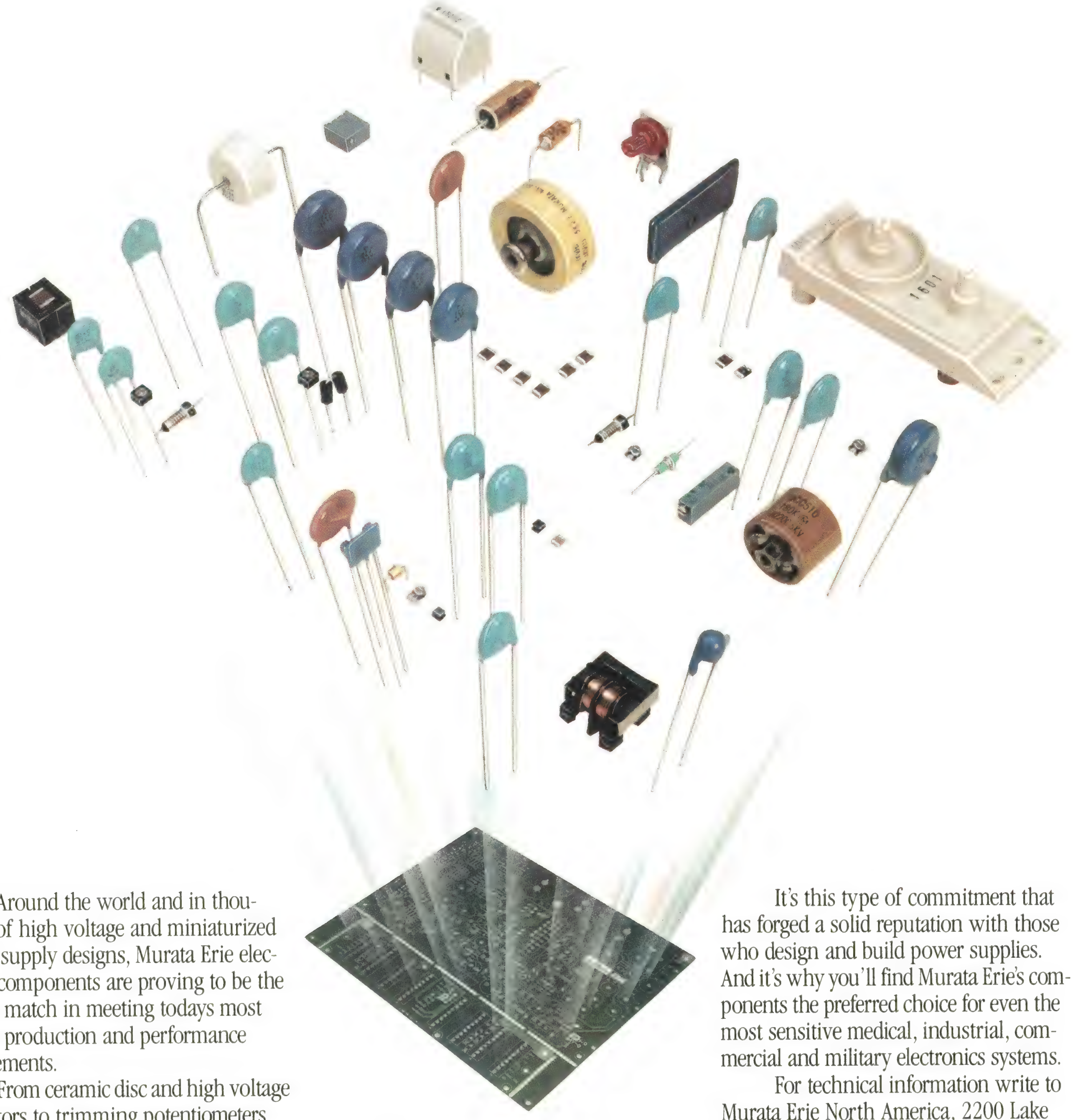

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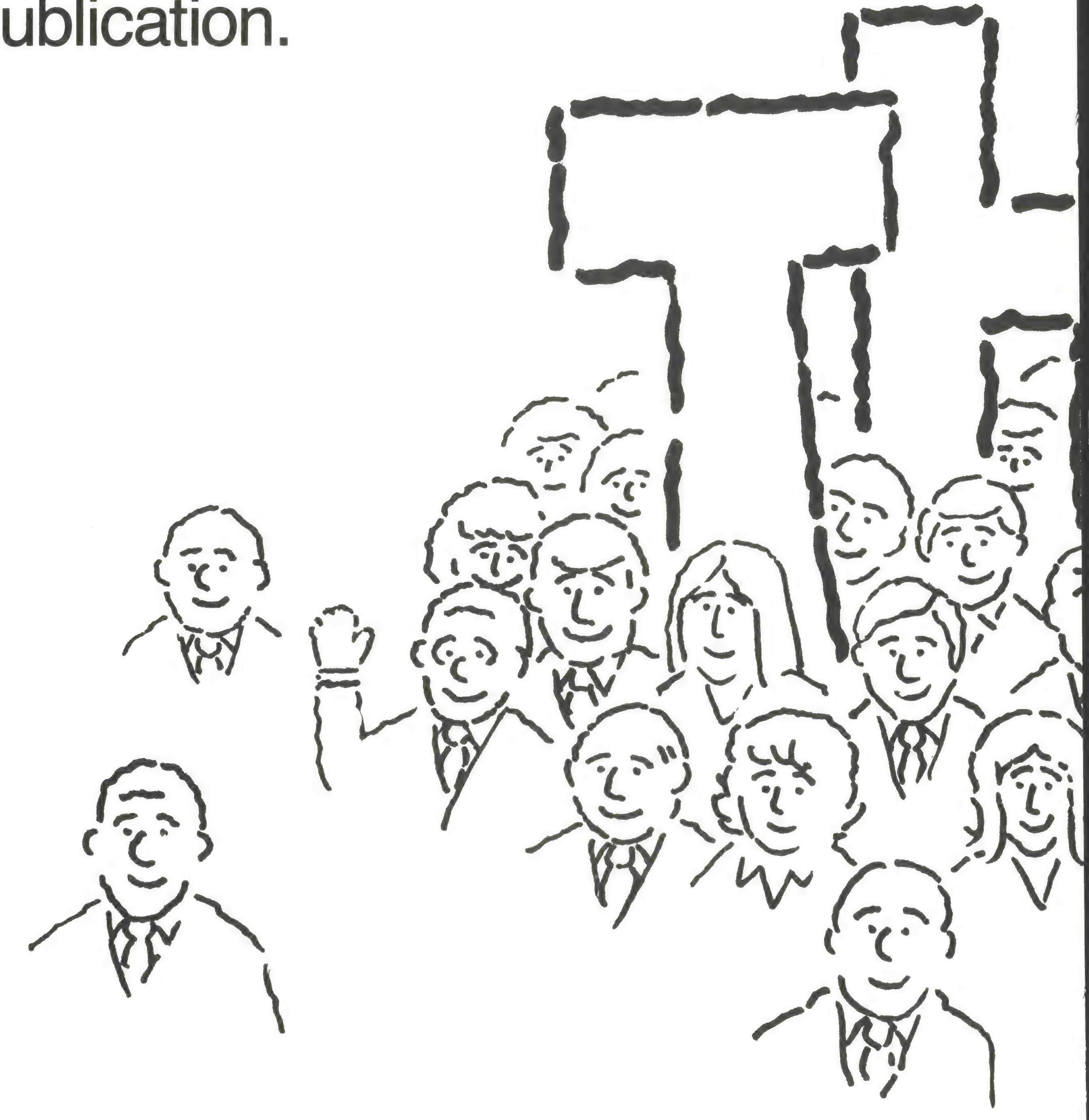

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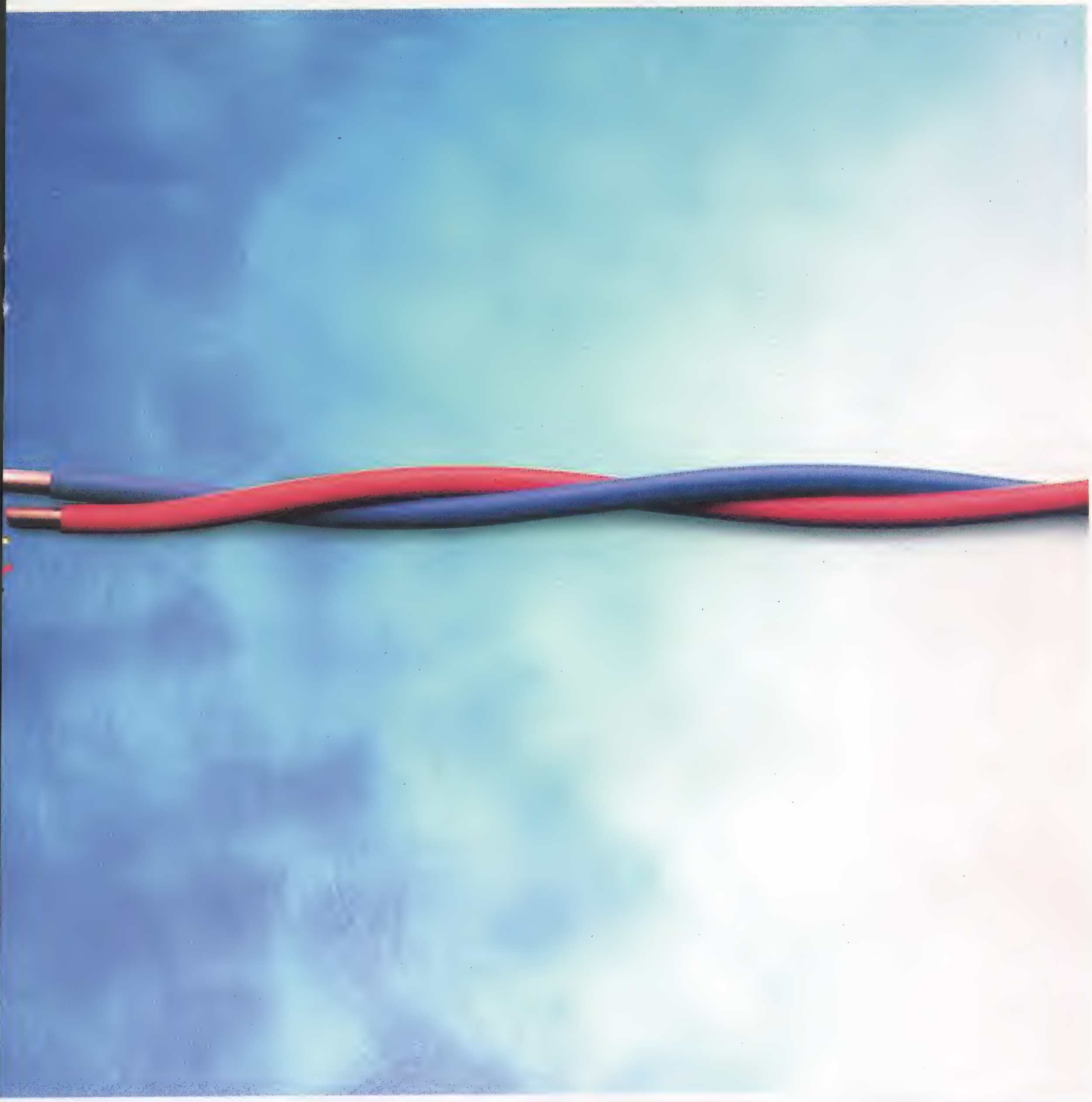

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LINEAR TECHNOLOGY

DESIGN NOTES

Number 33 in a series from Linear Technology Corporation April, 1990

Powering 3.3V Digital Systems

Dennis O'Neill

The new generation of high density digital devices requiring 3.3V power supplies impose some unique constraints on power supply designers. In nearly all cases the computers using these devices already have a 5V system supply. Deriving the 3.3V supply from the existing 5V rail permits system upgrades with a simple on-card solution. In many cases the 5V rail is the only supply available, mandating this approach. The first decision to be made is whether to use a switching regulator or a linear regulator? Switchers have a clear efficiency advantage when there is a large difference between the input and output voltage, but that advantage diminishes as the input voltage approaches the output voltage.

Simple calculations show that the efficiency of a switcher is marginally better in this application. Assuming a nominal input voltage of 5.0V and an output voltage of 3.3V, the efficiency of a linear regulator, (LT1083 type Figure 1A), independent of output current, is simply 3.3V/5.0V = 66%. For a switcher (Figure 1B) the efficiency is tougher to calculate. With only 5V available a PNP switch must be used, a MOSFET is not practical due to its gate drive requirements. The average inductor current will be equal to the load current. The duty cycle is determined by:

$$DC = (V_{OUT} + V_D)/(V_{IN} - V_{SAT} - V_D)$$

where $V_{OUT} = 3.3V$, $V_{IN} = 5.0V$, $V_{SAT} = V_{CE}$ sat. of Q_S, V_D = forward voltage of D1.

Assuming V_{CE} sat. of Q_S to be 0.6V at a forced Beta of 10 and the forward voltage of D1 to be 0.6V, (using a Schottky diode; a silicon diode would be closer to 1V at rated current), the formula indicates an 80% duty cycle. Significant power losses are listed below.

Switch Saturation Voltage	(0.6V) (1.0A) (80%) = 0.48W
Switch Base Current	(5.0V) (0.1A) (80%) = 0.40W
Diode Forward Voltage	(0.6V) (1.0A) (20%) = 0.12W
Inductor Voltage	(0.1V) (1.0A) (100%) = 0.10W
Switching Transients	≈0.10W
R_{SENSE} Voltage	(0.1V) (1.0A) (80%) = 0.08W
P.W.M. Circuit	(5.0V) (0.02A) (100%) = 0.10W
	1.38W

The efficiency is Power Out/Power In = 3.3W/(1.38W + 3.3W) ≈70%. This says that the switcher could be more efficient, but by a small margin (4%). Other considerations, such as noise filtering, further decrease the switchers efficiency. In addition, circuit design becomes complex. For example, short circuit sensing in the emitter lead of Q_S might require generating another supply greater than 5V to power the sense amplifier. Also, some form of adaptive base drive is needed to maintain efficiency at light loads.

When the small efficiency gain of a switcher is balanced against the advantages of a linear regulator (superior transient response, low noise, and ease of design) it becomes clear that the linear regulator is the best choice in this application.

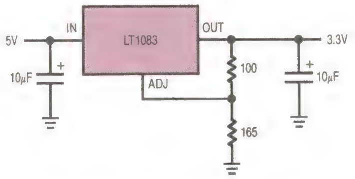


Figure 1A. Linear Regulator

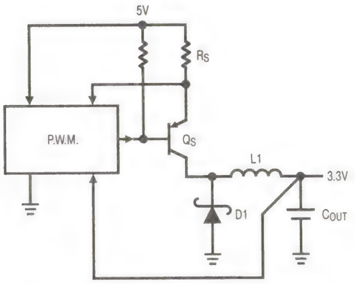


Figure 1B. Buck Switching Regulator

Regulator Design

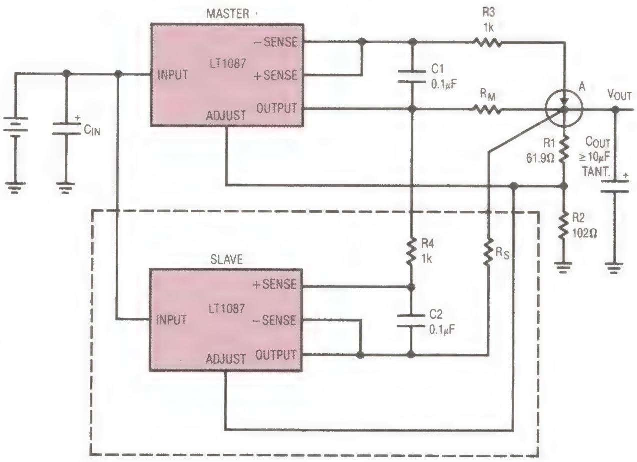
Figure 1A shows a basic linear regulator circuit utilizing an LT1083 adjustable low dropout regulator. These devices, specified for dropout voltage at several points over their operating current range, are ideal for this application. Nominal tolerance on the 5V rail in most systems is ±5% (4.75V to 5.25V). If the regulator dropout voltage is at the upper extreme of its specification (1.5V at maximum current and temperature for LT1083 family) it would still be able to supply 3.25V to the memory devices when the 5V rail is at the low end of its specification (4.75V). This is well within the allowable digital supply voltage range of 3.3V±10% (3.0V-3.6V).

LT1083 family behavior in dropout is benign. Once the device enters dropout the output simply follows the input. There is no increase in quiescent current during dropout as is common in PNP type regulators. The basic regulator circuit shown in Figure 1A supplies currents up to 7.5A. The device has all the normal protection features associated wth high current supplies, such as thermal and short circuit protection.

At currents greater than 7.5A several LT1087's are used in parallel (Figure 2). The LT1087 is the newest member of the LT1083 family. The device is a version of the LT1084 with two additional sense pins and is available in a 5-pin TO-220 package. When tied together the sense pins are used to Kelvin sense the output voltage. When used separately they form the inputs to a differential amplifier whose output changes the devices 1.2V reference voltage.

In Figure 2 the master LT1087's sense pins are tied together and connected to point A. This device senses and controls the output voltage using the Kelvin sense feature. R3 and C1 filter the voltage fed back to the sense pins. At low frequencies the output pin voltage of the master LT1087 is forced positive by the internal loop to maintain point A at the desired 3.3V value. This voltage is set by the ratio of R2/R1 according to the formula in Figure 2. The voltage across R_M is proportional to the load current.

The slave unit operates differently. This device senses the voltage across R_M and adjusts the voltage across R_S to be equal, effectively forcing this device to output a current equal to the master unit. The differential gain from the sense pins to the output is low (11), so to make the devices share current equally, R_M and R_S need to be scaled $R_M/R_S = 1.0/0.9$. R4 and C2 filter the feedback to the slave unit. The minimum load current for the total circuit is 10mA per device. R1 and R2 can be scaled to guarantee that the minimum load current spec will be met, and minimizes the output voltage error due to the adjust pin currents (50µA per device). The 10µF output capacitor is the minimum value needed to ensure stability. Larger output capacitors will improve transient response. R_M and R_S are chosen so that the voltage drop across them, at full load current (5A per device) is 40mV. This value is chosen to be large enough to ensure proper current sharing without significantly degrading dropout voltage. As noted in Figure 2, R_M and R_S will be in the 7mΩ-8mΩ range. These values are small enough to be made from either short lengths of wire or from carefully laid out PC traces. The absolute value of these resistors is not critical, but the ratio of R_M:R_S should be maintained.



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$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

Figure 2. High Current 5V-3.3V Regulator

The circuit as shown will source 10A. This capability can be increased, in increments of 5A, by duplicating the slave unit and properly sizing R1 and R2 to sink the additional 10mA per device. $C_{OUT'S}$ value may require adjustment upwards to maintain optimum transient response.

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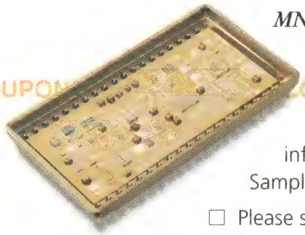

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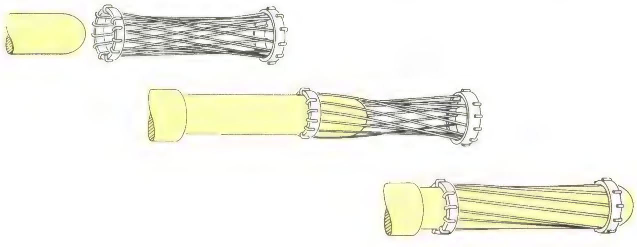

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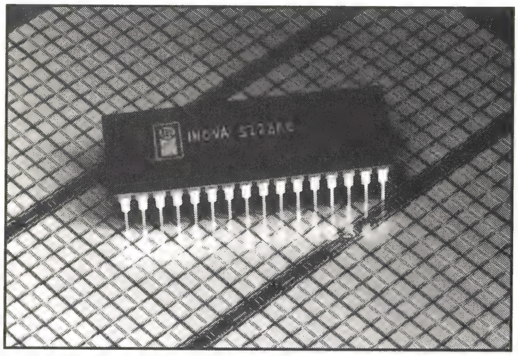

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S128K8-100	128K x 8	100ns	32-pin DIP	M,I,C
S128K8-120	128K x 8	120ns	32-pin DIP	M,I
S128K8L-55	128K x 8	55ns	32-pin DIP	I,C
S128K8L-70	128K x 8	70ns	32-pin DIP	M,I,C
S128K8L-85	128K x 8	85ns	32-pin DIP	M,I,C
S128K8L-100	128K x 8	100ns	32-pin DIP	M,I,C
S128K8L-120	128K x 8	120ns	32-pin DIP	M,I

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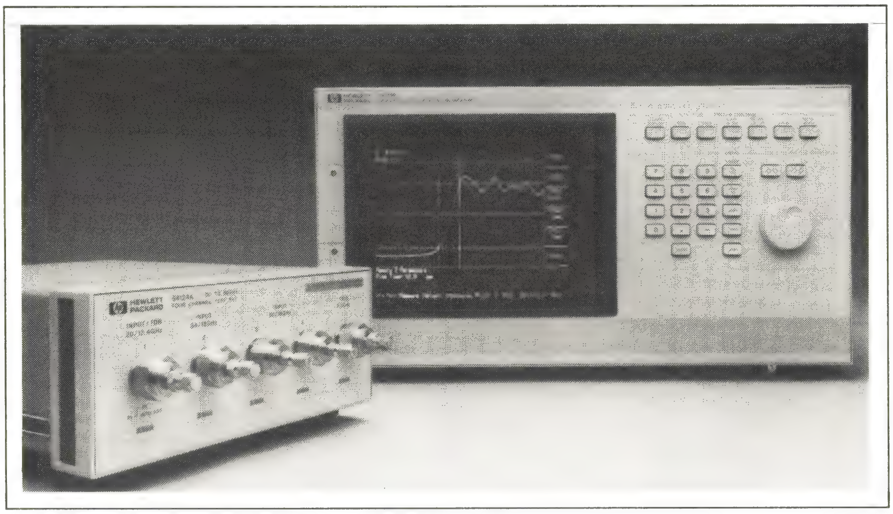

The 54124T digital storage oscilloscope (DSO) is the first such instrument to offer an analog bandwidth of 50 GHz. It does so on two of its four channels; the other two channels have bandwidths of 34 and 20 GHz. The scope also performs differential time-domain reflectometry; but unlike competitive instruments that offer this capability, this instrument uses only one pulse generator. It thereby avoids errors that can result from skew between the opposite-polarity outputs of a pair of generators. Optional accessories include a trigger module that operates to 18 GHz on sine waves, logic signals, and pulsed RF, and a 22-nsec delay line that lets you view the trigger event. $42,800. Delivery, 12 weeks ARO.

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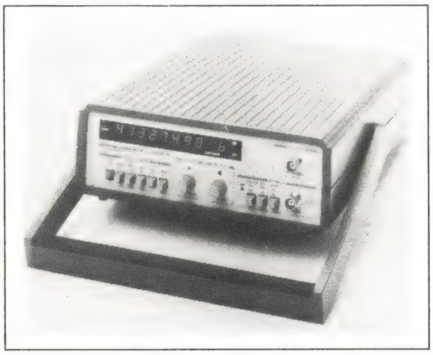

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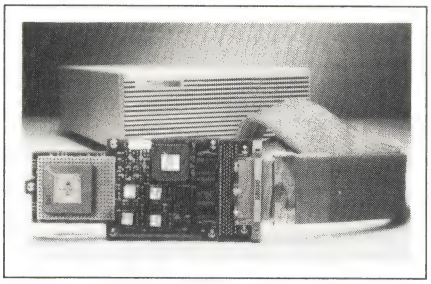
Micro Computer Control Corp, Box 275, Hopewell, NJ 08525. Phone (609) 466-1751. FAX (609) 466-4116. **Circle No. 367**



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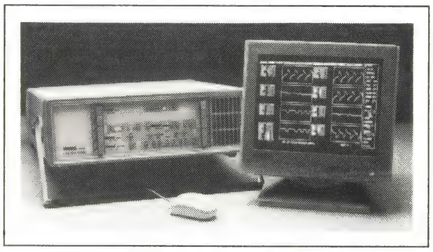

Analytek Ltd/Tektronix, 10261 Bubb Rd, Cupertino, CA 95014. Phone (800) 835-9433; (408) 725-2560. FAX (408) 725-8562. **Circle No. 370**

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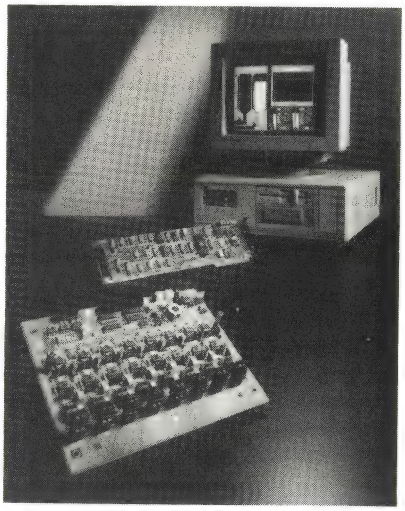

Analog Devices Inc, 1 Technology Way, Norwood, MA 02062. Phone (800) 426-2564.

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Arbitrary-Waveform Creator/Generator

- *Lets you use a mouse to define waveforms*
- *Stores a 16k-point × 12-bit waveform definition*

The IBM PC-based R4010 creates and generates arbitrary waveforms. You use a mouse to visually define your waveform or to edit acquired waveforms stored on disk. The generator will then reproduce the waveform with 12-bit resolution and programmable amplitude to 10V p-p. The instrument stores 16k waveform points and supplies the stored data to its DAC at speeds as high as 10M points/sec. The R4010 produces an output continuously or in bursts, and operates at fixed or swept frequencies. A disk containing a library of standard waveforms, including telephone sounds, comes with the generator. $2995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. FAX (206) 548-0322.

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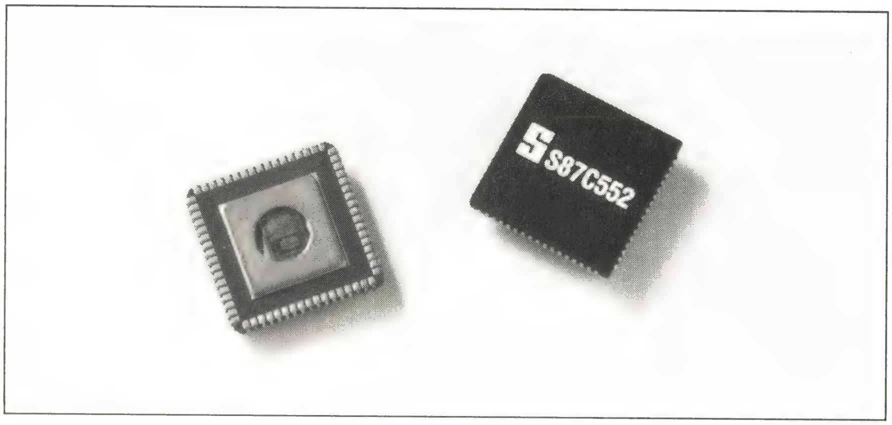
- *Includes multiple functions*
- *Highly integrated 80C51 derivative*



The 87C552 microcontroller is intended for real-time embedded control in automotive engine, instrumentation, and telecommunications applications. In addition to two PWM outputs, the µC features the two standard counter/timers of the 80C51, an additional timer with four capture registers and three 16-bit compare registers, a watchdog timer, a full-duplex UART, and a serial I^2C interface. The device also contains 8k×8-bit EPROM and an 8-channel, 10-bit ADC with a 50 µsec conversion time. The I^2C serial port is a 2-wire bus that supports device addressing and runs at 100k bits/sec. You can program the 80C51-compatible UART for baud rates to 1M bit/sec. The 87C552 is available in low-volume production quantities in a one-time-programmable EPROM version for less than $25; it is also available in a 68-pin windowed ceramic LCC package.

Philips Components-Signetics, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No. 383

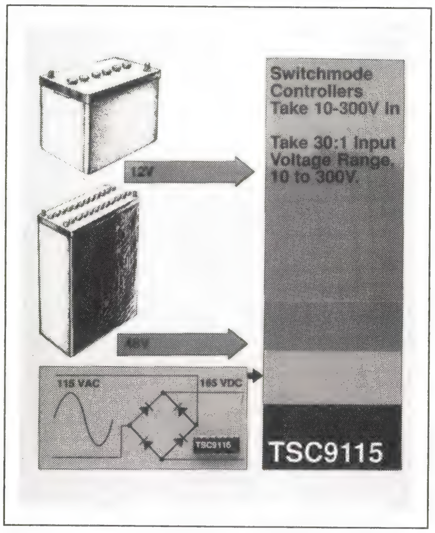
Video Shift Register

- *Has clock rates of 30 and 40 MHz*
- *Contains four 9-bit-wide shift registers*

The L64212 high-speed video shift register offers a choice of either 30- or 40-MHz clock rates. The primary advantage of these high clock rates is the register's ability to process 1k×1k-pixel images in real time at video rates. At a 30-Hz frame rate, a 1M-pixel image has a pixel rate of more than 30 MHz. The L64212 consists of four 9-bit-wide shift registers, each of which you can program for any length between 11 and 1035 words (pixels). You can configure the device as two line delays of 2070 pixels in length or as a single shift register of 4140 pixels in length. A circular buffer mode lets the circuit read a bank of data into memory and then continuously read out the data in a circular fashion. In a 95-lead ceramic pin-grid array: 30-MHz version, $175; 40-MHz version, $227 (100).

LSI Logic Corp, 1551 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 433-7593.

Circle No. 384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TSC9116
TSC9115

Switch-Mode Controller

- *Has 10 to 300V input range*
- *Implements popular SMPS topologies*

The TSC9115/9116 switch-mode controller, which features an input voltage range of 10 to 300V, is designed for use with single-ended, current-mode SMPS (switch-mode power supply) topologies. These topologies include buck, boost, Cuk, flyback, and forward converters. The wide input range is useful in applications using both batteries and off-line ac power. Other features include automatic start-up, which operates with only 1 mA of quiescent current, and the ability to self-power from an output. Available with inverting (TSC9116) or noninverting (TSC9115) outputs, these ICs include on-chip drivers that can drive power MOSFETs to 50W output. The devices are pin compatible with the Si9115/9116. In 16-pin DIPs or SOICs, $2.74 (10,000).

Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (800) 888-9966.

Circle No. 385

Differential Line Receiver

- *High common-mode rejection*
- *Has low audio-bandwidth distortion*

The SSM-2141 is a differential amplifier intended to receive inputs from a 600Ω balanced line in audio applications requiring low distortion and high common-mode rejection. Typical THD over the full

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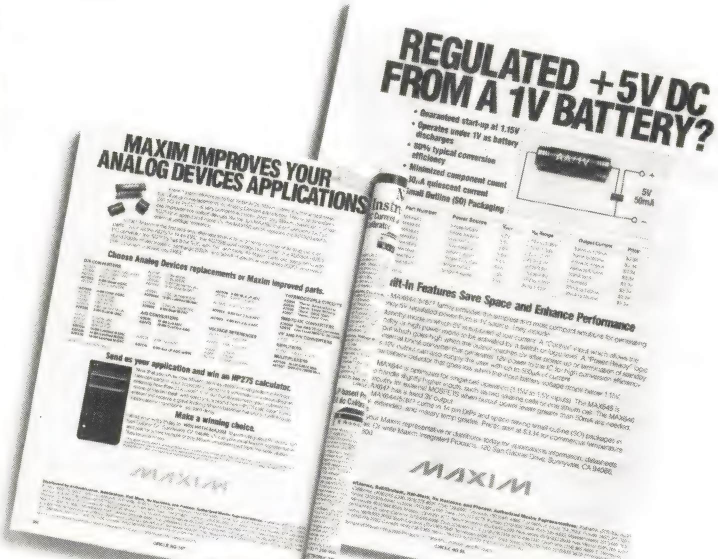

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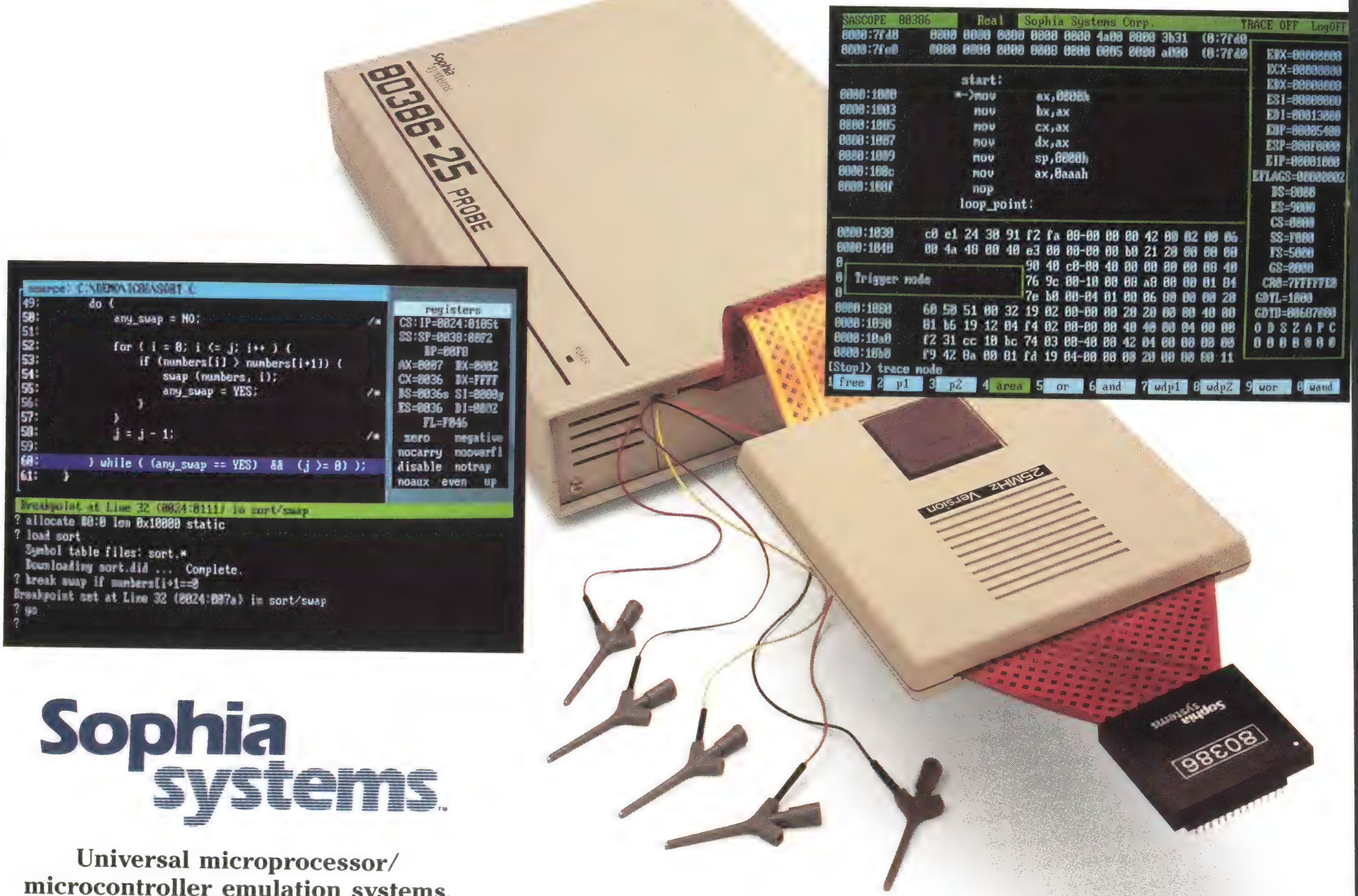

```
source: C:\DEMO\C86\SORT.C
        do {
            any_swap = NO;                               /*

            for ( i = 0; i <= j; i++ ) {
                if (numbers[i] > numbers[i+1]) {
                    swap (numbers, i);
                    any_swap = YES;                      /*
                }
            }
            j = j - 1;                                   /*

        } while ( (any_swap == YES)  &&  (j >= 0) );
    }
```

```
    registers
CS:IP=0024:0105t
SS:SP=0038:00F2
     BP=00F0
AX=0007  BX=0002
CX=0036  DX=FFFF
DS=0036s SI=0000g
ES=0036  DI=0002
     FL=F046
 zero     negative
nocarry   nooverfl
disable   notrap
noaux  even   up
```

```
Breakpoint at Line 32 (0024:0111) in sort/swap
? allocate 00:0 len 0x10000 static
? load sort
  Symbol table files: sort.*
  Downloading sort.did ...  Complete.
? break swap if numbers[i+1==0
Breakpoint set at Line 32 (0024:007a) in sort/swap
? go
?
```

```
SASCOPE  80386      Real    Sophia Systems Corp.                       TRACE OFF  LogOFF
0000:7fd8     0000 0000 0200 0000 0000 4a00 0000 3b31  (0:7fd0
0000:7fe0     0000 0000 0000 0000 0200 0005 0000 a000  (0:7fd0    EBX=00000000
                                                                   ECX=00000000
                 start:                                            EDX=00000000
0000:1000        *->mov      ax,0000h                              ESI=00000000
0000:1003           mov      bx,ax                                 EDI=00013000
0000:1005           mov      cx,ax                                 EBP=00005400
0000:1007           mov      dx,ax                                 ESP=000F0000
0000:1009           mov      sp,0000h                              EIP=00001000
0000:100c           mov      ax,0aaah                           EFLAGS=00000002
0000:100f           nop                                             DS=0000
                 loop_point:                                        ES=9000
                                                                    CS=0000
0000:1030    c0 e1 24 30 91 f2 fa 00-00 00 00 42 00 02 00 06        SS=F000
0000:1040    00 4a 48 00 40 e3 00 00-00 00 b0 21 20 00 00 00        FS=5000
0             90 40 c0-00 40 00 00 00 00 00 40                      GS=0000
0  Trigger mode               76 9c 00-10 00 08 a8 00 00 01 04     CR0=7FFFFFE0
0                             7e b0 00-04 01 00 06 00 00 00 20     GDTL=1000
0000:1080    60 50 51 00 32 19 02 00-00 00 20 20 00 00 40 00      GDTB=00607000
0000:1090    81 b6 19 12 04 f4 02 00-00 00 40 40 00 04 00 00      O D S Z A P C
0000:10a0    f2 31 cc 10 bc 74 03 00-40 00 42 04 00 00 00 00      0 0 0 0 0 0 0
0000:10b0    f9 42 8a 00 01 fd 19 04-00 00 00 20 00 00 00 11
[Stop]> trace mode
1 free  2 p1  3 p2  4 area  5 or  6 and  7 wdp1  8 wdp2  9 wor  0 wand
```

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80386SX/376	16 MHz

NEC Microprocessors	
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V40/50	10 MHz
V25	16 MHz
V33	16 MHz
V60	16 MHz

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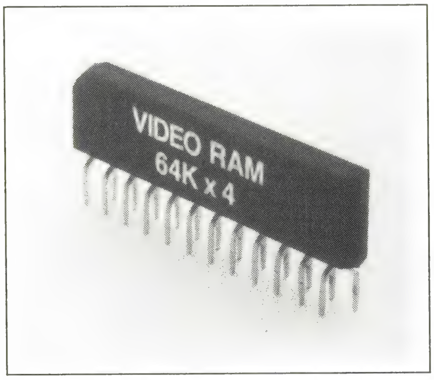
CIRCLE NO. 114

audio bandwidth is 0.01% into a 600Ω load and 0.001% into a 100 kΩ load. Common-mode rejection is typically 100 dB at dc and 70 dB at 20 kHz. Other specifications include a slew rate of 9.5V/μsec and a −3-dB bandwidth of 3 MHz. The device operates over the −40 to +85°C industrial temperature range and comes in an 8-pin plastic DIP. $1.95 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. FAX (408) 727-1550. **Circle No. 386**



Multiport Video RAM

- *Contains two read/write memories*
- *Zig-zag in-line package*

The GM53C261 is a multiport video RAM optimized for use in PC graphics and workstations requiring high-speed serial data. The low-power CMOS device contains two read/write memories; a 256×4-bit serial-access memory, and a 64k×4-bit RAM. Although the memories communicate with each other over an internal bus, they can also operate independently and serve two operations simultaneously. The chip's architecture is structured for efficient performance in bit-mapped graphics systems. With its two asynchronous memories, the device eliminates the usual contention problem between the screen-update and screen-refresh functions. The CPU performs update operations on the RAM, which acts as a frame buffer, while the serial-access memory serially transforms pixel information to the monitor. The device comes in a plastic, zig-zag in-line package for use in high-density boards. $5 (100).

Goldstar Technology, 3003 N First St, San Jose, CA 95134. Phone (408) 432-1331. FAX (408) 432-6053. **Circle No. 387**

Low Dropout Regulator

- *Rated at 5A*
- *Features remote sensing*

Rated at an output current of 5A, the LT1087 can operate down to a 1V input-to-output differential. This dropout voltage is fully specified and guaranteed as a function of load current over the full output-

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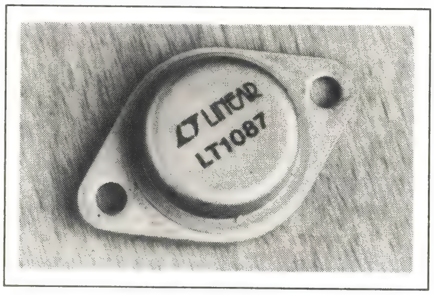


current range of the device. The regulator's reference voltage is trimmed to 1%; current limiting minimizes stress on the regulator under overload conditions. Line regulation is 0.05%, and load regulation is 0.1% at the sense point. The regulator features remote sensing, which can eliminate load regulation errors caused by voltage drops in the wires connecting the regulator to the load. Available in a 4-pin TO-3 metal can or a 5-pin TO-220 plastic package, from $4.45 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545. FAX (408) 434-0507. **Circle No. 388**

100-MHz Video Amplifier In Die Form

- *Features dielectric isolation*
- *Has high-current output*

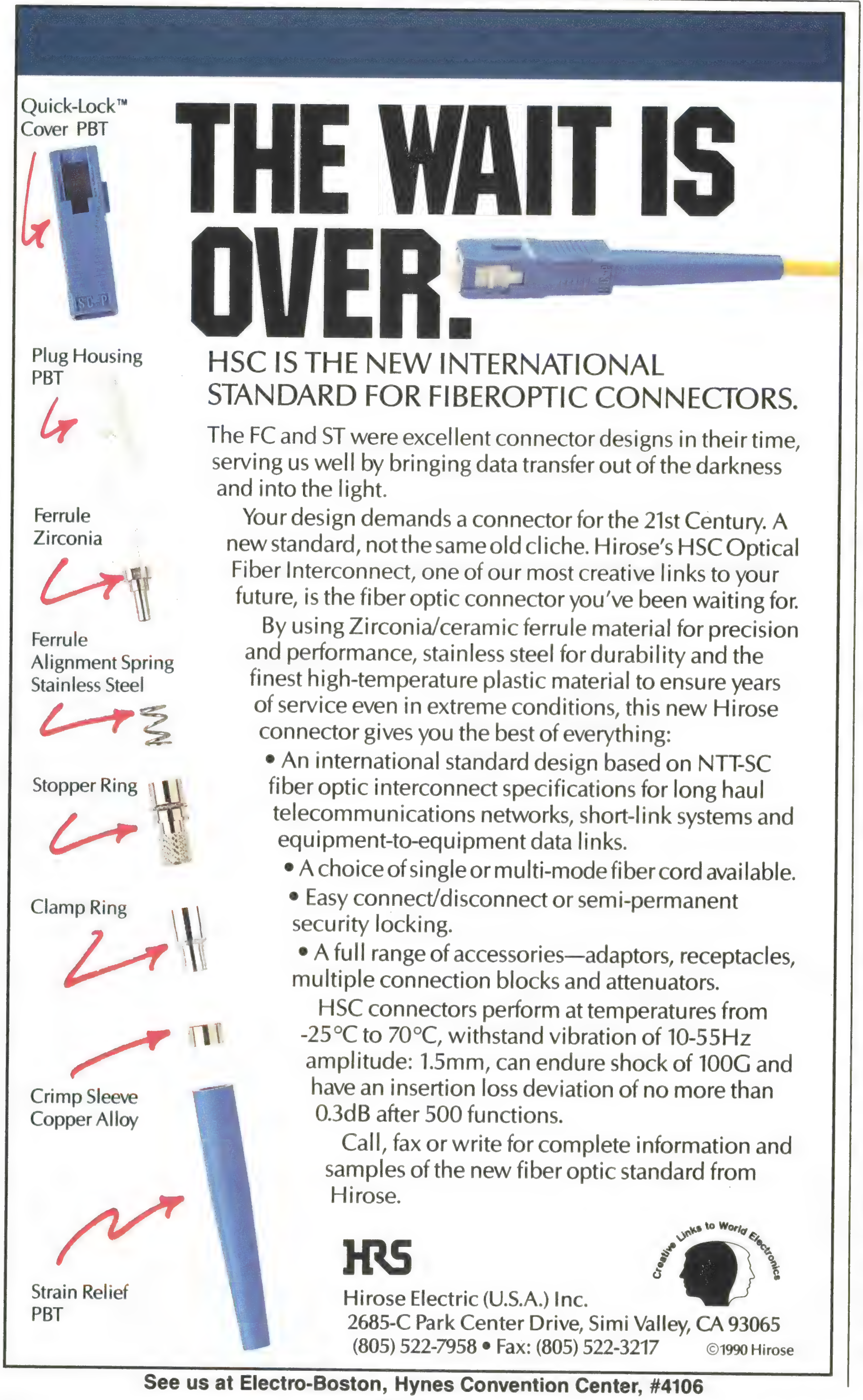
The CA2003, which features dielectric isolation in the fabrication process, is now available in die form for hybrid applications. In addition to its 100-MHz unity-gain bandwidth, the amplifier chip also features an output current of ±230 mA. The CA2003 contains a high-impedance input amplifier, a complementary-output power stage, and a current limiter to protect the output transistors. For higher output currents, you can use several devices in parallel without any current-sharing arrangements. $1.21 (100,000).

Calogic Corp, 237 Whitney Pl, Fremont, CA 94539. Phone (415) 656-2900. **Circle No. 389**

Dual-Architecture Static RAM

- *Has 35-nsec speed*
- *1M × 1-bit or 256k × 4-bit option*

Featuring a 35-nsec access time, the M5M551001 static RAM (SRAM) is configurable as either a 1M × 1-bit or 256k × 4-bit device. This dual architecture lets you stock only one device type and configure it as needed. When the configuration pin (pin #21) is tied to V_{CC}, the SRAM acts as a 1M × 1-bit device; when pin #21 is tied to ground, the result is a 256k × 4-bit device. For customers requiring an output-enable function, the company offers the 256k × 4-bit M5M51004 metal-mask option of the M5M51001. The static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RAMs are available in 28-pin, 400-mil plastic DIPs and SOJ packages. Active power requirements are 660 mW; standby power is 11 mW. In plastic DIPs, M5M51001, $195; M5M51004, $210 (100).

Mitsubishi Electronics, Semiconductor Div, 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900. FAX (408) 730-4972.

Circle No. 390

Dual Transceiver

- *Meets MIL-STD-1553B*
- *Operates from a 5V supply*

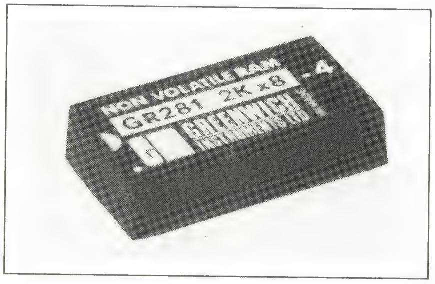
Featuring custom monolithic drivers and receivers, the CT2520 dual low-power MIL-STD-1553B transceiver operates from a single 5V supply. The hybrid design results in lower power dissipation at 100% duty cycle and 125°C case temperature. Each drive dissipates less than 1W at 25% duty cycle. Other features include ac interstage coupling to prevent static burnout, a filtered receiver to improve the S/N ratio of the system, and a typical output offset of 20 mV. The dual CT2520 is available in plug-in double DIP and flatpack configurations. The device operates over the −55 to +125°C military temperature range. From $315.

Marconi Circuit Technology, 45 Davids Dr, Hauppauge, NY 11788. Phone (516) 231-7710. FAX (516) 231-7923.

Circle No. 391

Nonvolatile Static RAM

- *Organized as 2k×8 bits*
- *Has 45-nsec access time*



Organized as 2k×8 bits, the GR281-4 is a nonvolatile CMOS static RAM (SRAM) with an access time of 45 nsec. The SRAM features a high-speed power-down circuit that, together with an integral lithium cell, retains data even if the external supply drops from 5V to zero in a time period as fast as 15 μsec. Because the device is self-contained, it can replace an ordinary SRAM, automatically changing the location to nonvolatile. The lithium cell retains memory for 10 years. The SRAM comes in a 24-pin DIP that is pin-compatible with 2716 EPROMs. £17.

Greenwich Instruments Ltd, The Crescent, Main Rd, Sidcup DA14 6NW, UK. Phone (1302) 4931. FAX (1302) 4933.

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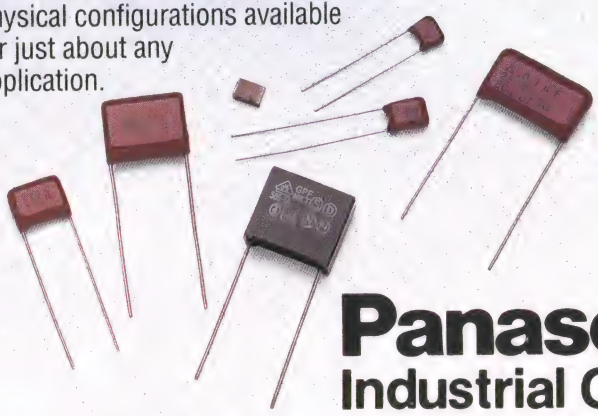
Quality is the first reason you'll specify Panasonic film capacitors. And you'll also be happy to know about the broad range of dielectric systems and physical configurations available for just about any application.



We're in Charge of Quality
Panasonic film capacitors meet rigorous quality assurance standards. They are the same high quality components used in Panasonic electronic products. We will never offer to sell a device we would not recommend for our own product lines.

We'll help you build exceptional quality and confidence into every circuit. Think Panasonic for all film capacitor requirements.

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CIRCLE NO. 116

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Central Regional Sales Office
425 East Algonquin Rd., Arlington Heights, IL 60005
Tel: (708) 981-4837 Fax: (708) 593-3794

Western Regional Sales Office
6550 Katella Ave., Cypress, CA 90630
Tel: (714) 373-7332 Fax: (714) 373-7323

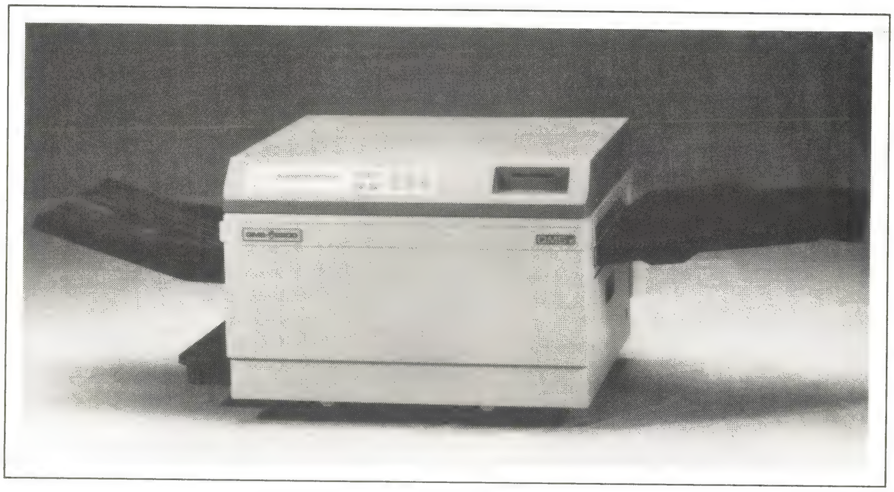
NEW PRODUCTS

COMPUTERS & PERIPHERALS

Postscript Laser Printer

- *Has 39 resident typefaces*
- *Can produce 20,000 pgs/month*

The QMS-PS 2200 Model B laser printer produces Adobe System's PostScript fonts. It prints in black and white at 22 pgs/minute on 8.5×11-in. sheets and at 11 pgs/minute on 11×17-in. sheets. Capable of producing 20,000 pgs/month, the PS 2200 operates from a 250-sheet paper cassette or from a 100-sheet paper bin. Its print controller has a 16.67-MHz 68020 μP, 4M bytes of RAM, 1M byte of ROM, and 39 resident PostScript typefaces. The printer has an RS-232C, an RS-422/AppleTalk, and a Centronics parallel interface. A SCSI port lets you attach as many as seven optional hard-disk drives. An optional communications controller, the PrintLink, lets you operate the printer using an Ethernet TCP/IP (transmission control protocol/internet protocol) network. The printer comes with PS Executive software as well as start-up, testing, and operation utilities. $9995.



QMS Inc, Electronic Publishing Group, 1 Magnum Pass, Mobile, AL 36618. Phone (800) 631-2692. FAX (205) 633-0013. **Circle No. 374**

Internetworking System

- *Has multiple LAN and WAN interfaces*
- *Uses AMD's 29000 RISC CPU as its primaryμP*

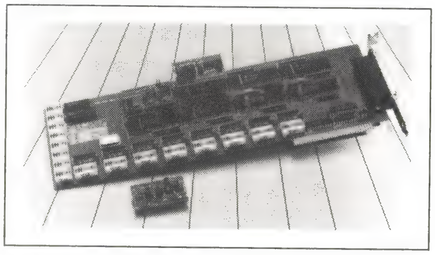
The LanNet Express is an internetwork communications system for multiple LANs and WANs (wide-area networks). The system uses a multiple μP design, which has an AMD 29000 RISC (reduced-instruction-set computer) μP as its primary CPU and multiple Motorola 56001 μPs as I/O processors. A 32-bit bus architecture operates at a 230M-bps data-throughput rate. The processing power allows the system to filter more than 75,000 packets/sec and forward more than 30,000 packets/sec in an Ethernet IEEE-802.3 internetworking application. The system handles data rates as fast as 10M bps on its six LAN ports and speeds as fast as 2.048M bps on its 12 WAN ports. The system's internodal protocol, ExpressLink, is compatible with a wide range of network topologies. The protocol transmits data on the network based on least-cost calculations and automatically reroutes data when line or facility outages occur. Basic system, $5890; typical configurations, $13,995 to $25,000. Delivery, 90 days ARO.

Racal-Milgo, Box 407044, Fort Lauderdale, FL 33340. Phone (305) 846-1601. FAX (305) 846-4942. TWX (510) 955-4145. **Circle No. 375**

Multiple Serial Communicator

- *Plugs into an IBM PC-compatible computer*
- *Provides eight serial communications channels*

The MCS-8 provides eight serial-communications channels on a single plug-in card for your IBM PC, PC/XT, PC/AT, or compatible computer. The protocol for each channel conforms selectively to RS-232C, RS-422, RS-485, or a 20-mA current loop, as preset by plug-in modules on the card. Dual in-line switches assign one of 128 addresses and a hardware interrupt line to each channel. Software drivers, 2-channel version, £195; 8-channel version, £495; fan-out cable that attaches to eight serial connectors, £45.



Blue Chip Technology, Hawarden Industrial Park, Manor Lane, Deeside, Clwyd, UK. Phone (0244) 520222. FAX (0244) 531043. TLX 61471. **Circle No. 376**

80386 Single-Board Computer

- *Measures 5.75×8 in.*
- *Operates from 0 to 70°C and consumes 10W from 5V*

The Little Board/386 IBM PC/AT-compatible single-board computer (SBC) uses a 20-MHz 80386 μP. Its

PANASONIC SHARPENS THE LEADING EDGE IN POWER SUPPLY CAPACITOR TECHNOLOGY

Quality is the first reason you'll choose Panasonic capacitors. But you'll also appreciate our innovative designs that give you cost-effective, space saving benefits. And our wide selection of lytic, film and ceramic capacitors lets you specify exactly the right component for your power supply application.

We're in Power for Quality

Panasonic capacitors meet rigorous quality assurance standards. They are the same high quality components used in Panasonic electronic products. We will never offer to sell a device we would not recommend for our own product lines.

We offer several types of TS series aluminum electrolytic capacitors in a wide range of case size options for input filter applications requiring high temperature–high ripple current capability. Our HFQ and HFZ miniature radial lytics are ideally suited for output filter applications. They offer long life and exceptionally low impedance. Our ECQ series of film caps and NS series of ceramic caps are effective interference suppressors and are safety agency approved for across-the-line and line-to-ground applications. For pure power, call the nearest Panasonic sales office today.

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Western Regional Sales Office
6550 Katella Ave., Cypress, CA 90630
Tel: (714) 373-7332 Fax: (714) 373-7323

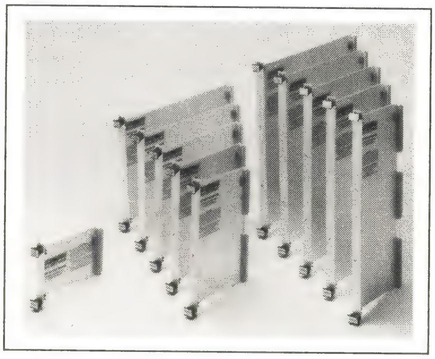
5.75×8-in. surface area covers the same size surface area as that of a half-height 5¼-in. disk drive. Designed for embedded applications, the SBC contains as much as 4M bytes of RAM, a floppy-disk controller, a battery-backed real-time clock, dual RS-232C ports, a parallel printer port, and an optional SCSI port. Little Board/386 has an IBM PC/AT-compatible bus header for system expansion and a daughter-board carrier for an 80387 coprocessor. The SBC operates over a range of 0 to 70°C and consumes 10W from a 5V power supply. The board is 100% mechanically compatible with the company's other Little Boards. The company offers a series of expansion modules such as IBM VGA, CGA, EGA, and LCD controllers; a 2400-baud modem; and a LAN interface. In addition, the board has sockets to implement solid-state disks. $1170 (100) without RAM.

Ampro Computers Inc, 1130 Mountain View/Alviso Rd, Sunnyvale, CA 95089. Phone (408) 734-2800. TLX 4940302. FAX (408) 734-2939. **Circle No. 377**

VMEbus Slot-Bypass Boards

- *Bypass control signals for daisy-chain format*
- *Front-panel aluminum card provides RFI shielding*

The Slot-Bypass-Board family of products fills spare slots in VMEbus or SUNbus backplanes. The VME-style front panels have card ejectors; the panels attach to aluminum cards with VME connectors. The boards come in 3U, 6U, and 9U Eurocard formats with one, two, and three VME connectors, respectively. The aluminum boards provide RFI shielding, and a male DIN connector, mounted on the rear of one of the VME connectors, lets you bypass signals on the bus. For example, you can bypass the Bus Grant and Interrupt Acknowledge signals to daisy-chain these control signals to other boards on the bus. In addition, the board maintains integrity of the air flow system. 6U160, $19.95 (100).



Dawn VME Products, 47073 Warm Springs Blvd, Fremont, CA 94539. Phone (415) 657-4444. FAX (415) 657-3274. **Circle No. 378**

VMEbus Single-Board Computer

- *Accommodates four 88100 CPUs and eight 88200 CMMUs*
- *Has two SCSI ports and a 32-bit Ethernet controller*

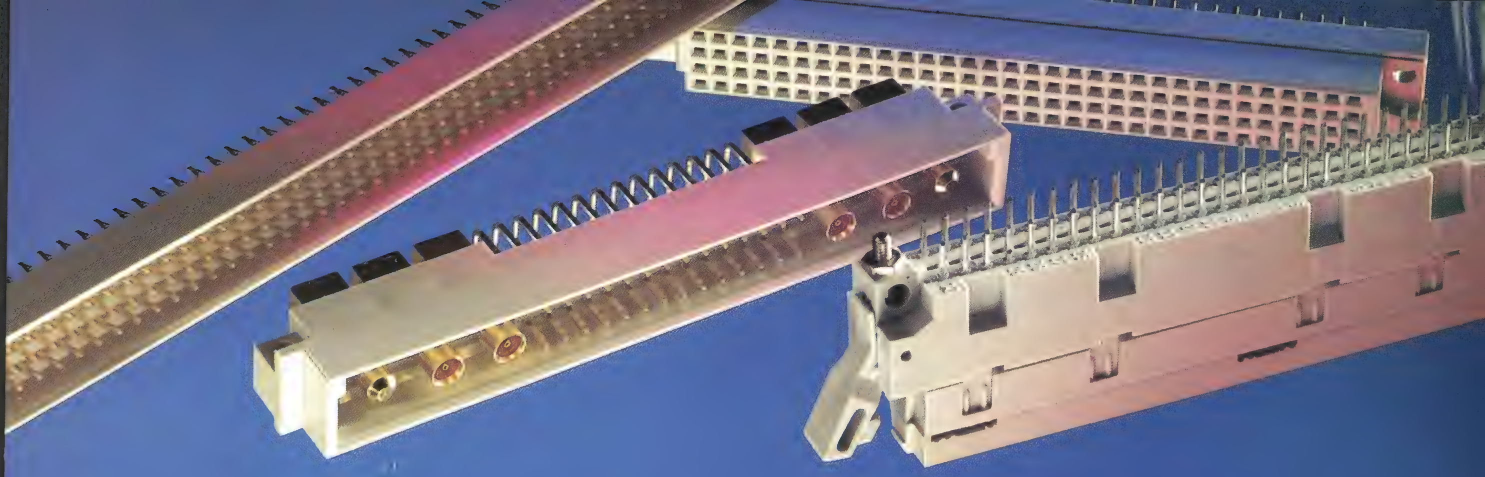
The TP882V single-board computer for VMEbus systems accommodates as many as four 88100 CPUs and eight 88200 CMMUs (cache controller and memory-management unit) on a single mezzanine card. The combination delivers as much as 110 VAX MIPS. The device features dual SCSI controllers and a 32-bit Ethernet controller, which has a 32-bit DMA controller that transfers data between an Ethernet network and its main memory. Other features include master or slave interfaces, 256k bytes of EPROM, and a battery-backed real-time clock. The TP882V has four serial communications ports that you can configure to include two asynchronous or synchronous ports with DMA, two RS-232C, RS-422, or V.35 ports, and one LocalTalk mode port. The device's CPUs, memory, VME, and I/O interfaces connect to a high-speed bus for fast data transfer. 20-MHz version with one CPU and two CMMUs, $10,000.

Tadpole Technology Inc, 1601 Trapelo Rd, Waltham, MA 02154. Phone (617) 890-8898. FAX (617) 890-7573. **Circle No. 379**

Computer Input Device

- *Consists of miniature mouse inside head of a pen*
- *Has PS/2 mouseport connector*

The MousePen input device for IBM PC, PC/XT, PC/AT, PS/2, and compatible computers consists of a miniature mouse located inside the head of a pen. It has two input buttons and comes with drivers that operate with any program that employs a Microsoft mouse. The device also features a PS/2 mouseport connector and a single adapter that accommodates both DB9 and DB25 serial ports. Other features include pop-up menus for Lotus 1-2-3, dBASE III, and WordPerfect along with documentation for developing custom menus for specific applications. TelePaint, a color-paint program that operates in IBM VGA mode is included in the package. The MousePen fits into a pocket or attache case and writes on any surface. It has a resolution from 50 to 1000 pulses/in. and a tracking speed of 18 ips. The device measures



PANDUIT® *HI-CON*™ EUROCARD CONNECTORS

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In breadth of line.
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In reliability.
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In service and support.

The wide variety of PANDUIT DIN connectors lets you choose just the connector that's best for your application. With a gold thickness in mating areas matched to your required performance level. And with excellent delivery—from stock to 2 weeks.

- Press-fit connectors with "Eye-of-the Needle" compliant design to minimize plated through hole stress and maximize performance.
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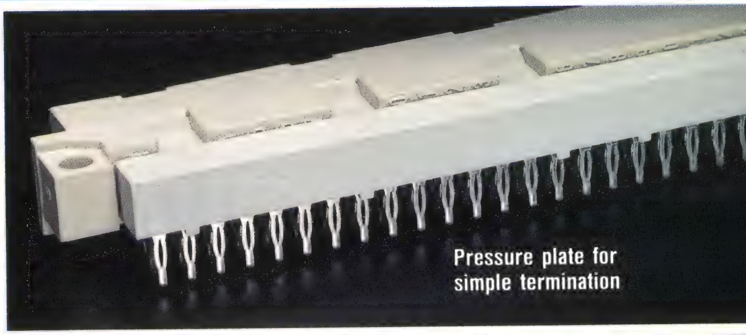
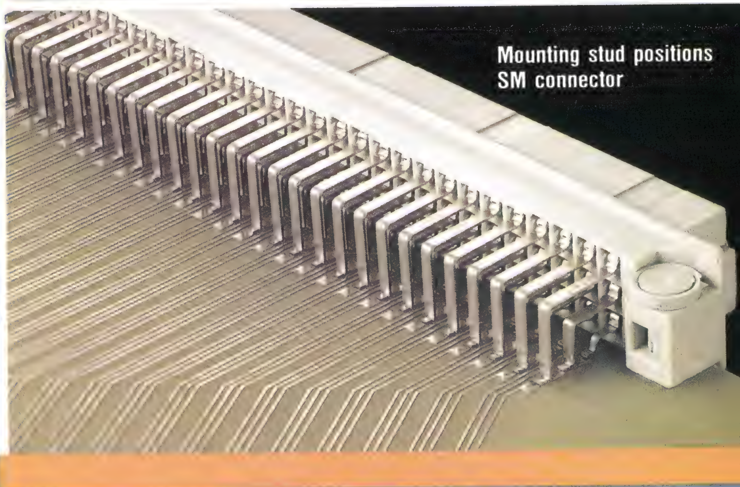
Call Connector Technical Service today, toll free 1-800-777-3300, ext. 4265.



Pressure plate for simple termination

Compliant design to eliminate hole deformation



Mounting stud positions SM connector

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CIRCLE NO. 118

Visit PANDUIT at ELECTRO '90 Booth 1920-27

6.1×0.6×0.7 in. and weighs 90g. $129.

International Machine Control Systems Inc, 1332 Vendels Circle, Paso Robles, CA 93446. Phone (805) 239-8976. FAX (805) 239-8978.
Circle No. 380

VMEbus Graphics Board

- *Uses TI's TMS34010 graphics μP*
- *Provides IBM VGA resolution and either 16 or 256 colors*

The DGC2 VMEbus graphics board uses TI's TMS34010 graphics processor. The all-CMOS board provides all standard IBM VGA resolutions and displays either 16 or 256 colors from a palette of 252,114 colors. Using an MC1378 composite-sync-generator IC, the board can mix an optional NTSC-compatible input signal with graphics overlays from the TMS34010. The 512k bytes of video RAM stores as many as four frames using 4 bits/pixel. You can optionally expand its 512k-byte program or data dynamic RAM to a maximum of 2M bytes in 512k-byte increments. Two onboard EPROM sockets store as much as 256k bytes of firmware. The μP-style instruction set lets you process graphics using the host's CPU or its onboard EPROMs. $2240 (100).

Dyantem, 15795 Rockfield Blvd, Suite G, Irvine, CA 92718. Phone (714) 855-3235. FAX (714) 770-3481.
Circle No. 381

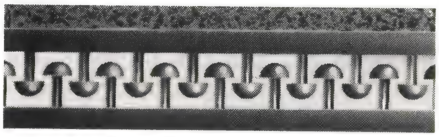
Counter/Timer Card

- *Five 16-bit channels with gate and clock inputs*
- *Generates a 1-MHz clock from system's 10-MHz clock*

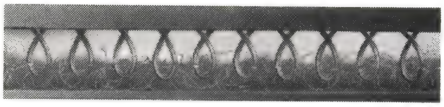
The WH-CNTT-5 counter/timer card for the company's WorkHorse programmable controllers features an AMD 9513A timer controller that provides five 16-bit timer/counter channels. The card has debounce-logic circuitry for five input-clock and five input-gate signals. The card generates its 1-MHz clock frequency from the system's 10-MHz clock signal. It has five optocouplers, which you can configure as input or output buffers. You can configure the counters to generate pulse, square-wave, or variable duty-cycle output waveforms. Each counter has a load register for loading the counter to a predetermined number and a hold register to save count values without disturbing the counter. WH-CNTT-5, $550; solid-state relay modules, $18.

Keithley MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179.
Circle No. 382

Faster fasteners for access panels.



Dual Lock™ brand Reclosable Fasteners



Scotchmate™ brand Hook and Loop Reclosable Fasteners

With 3M's reclosable fasteners, access panels and doors simply pull open and push shut. These fasteners have a strong, pressure sensitive adhesive backing for immediate attachment and long-term performance. They replace cumbersome and unsightly conventional fasteners, eliminating the need to drill holes and refinish surfaces. So production is faster, manufacturing costs less and access is easier.

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FREE SAMPLES. For more information and free samples of 3M fasteners, mail to 3M Industrial Specialties Division, 3M Center Bldg. 220-7E-01, St. Paul, MN 55144-1000.

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☐ Please have a sales representative call me. **EDN041290**

3M

Circle 126 For Sales Assistance

Circle 127 For Information

Two FAST OP AMPS

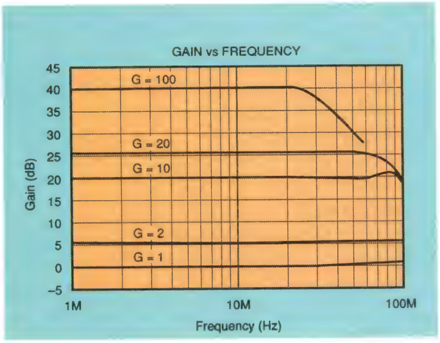
Constant Bandwidth, Wide Supply Range

Our new OPA603 current feedback design provides nearly constant bandwidth over a wide range of closed-loop gains and settles to 0.1% in 50ns.

If you need current feedback, you won't find a solution that's easier to implement. It's monolithic and features a standard op amp pinout. Simple curves in the product's data sheet help users quickly determine proper resistor feedback values. And OPA603's performance is guaranteed at both ±5V and ±15V.

- Bandwidth, 100MHz (G = 10)
- Output voltage, ±10V into 150Ω
- Output current, 150mA peak
- Differential gain, 0.03% @ 4.43MHz Differential phase, 0.025° @ 4.43MHz
- Settling time, 50ns to 0.1%
- Slew rate, 1000V/μs
- 8-pin plastic DIP

And, if you think all "classic" op amps have to be slow, check out our OPA620/621.



OPA603's bandwidth remains nearly constant over wide range of closed-loop gains.

Wide Bandwidth −80dB IMD (5MHz)

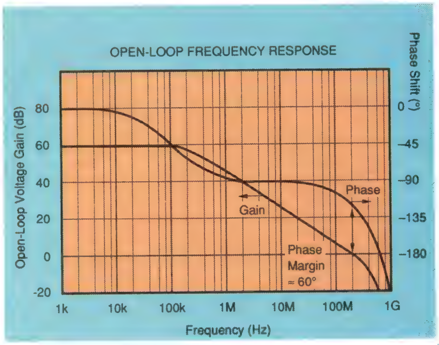
OPA620/621 gives designers exceptional speed, precision, and very low distortion in an economical monolithic design.

The "classic" voltage feedback architecture offers very low offset, fully symmetrical differential input.

OPA620 is unity-gain stable, settles fast and clean, and is usable over a wider range of gains. Choose our decompensated OPA621 for wider bandwidth in gains of two or greater.

- GBW, 200MHz, (OPA620) 500MHz, G = 2, (OPA621)
- Settling time, 25ns to 0.01%
- Slew rate,
  250V/μs (OPA620)
  500V/μs (OPA621)
- Output voltage, ±3.0V into 50Ω
- Offset voltage, ±100μV
- Differential gain, 0.05% @ 3.58MHz Differential phase, 0.05° @ 3.58MHz
- Noise, $2.3\text{nV}/\sqrt{\text{Hz}}$
- Plastic, ceramic, SOIC packages and die

Burr-Brown Corp.
P.O. Box 11400
Tucson, AZ 85734
U.S.A.



OPA620 provides outstanding gain/phase performance.

ONE SOLUTION

If you need a fast op amp, come to the leader, *Burr-Brown*. We have data sheets, application notes, and samples waiting for you. Contact your local sales office or
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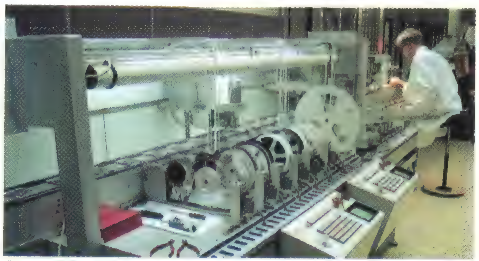
CIRCLE NO. 125

A 1983 concept that's still an innovation - Ericsson component power

If you've only just discovered the economy, reliability and flexibility of component power, don't worry. Even some power supply manufacturers think it's new!

In fact, component power concept - using very efficient, high frequency DC/DC converters as complete power 'components' for distributed power architecture - was introduced by Ericsson way back in 1983. And EriPower™ modules have since been proven in thousands of applications worldwide.

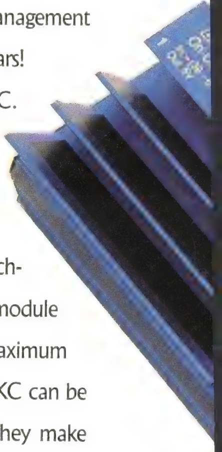


The PKA & PKC, DC/DC converters are produced on fully automated lines to guarantee consistently high quality and reliability

The first product, the PKA 25 to 40 Watt converter, set the standard and is still the market leader by far. Using hybrid construction and 300 kHz switching it's the world's smallest converter to offer full power operation at 85°C. And with ceramic capacitors for filtering and effective thermal management design, it has a demonstrated MTBF of over 200 years!

The PKC In-Card, 15-18 Watt DC/DC converters provide ultra low profile

This same concept applies to the 15 and 18 Watt PKC. With a footprint smaller than a credit card, these sub-miniature converters offer the unique option of In-Card low profile mounting. The mechanical design allows the center of the module to rest in a slot in the PCB, giving a maximum height of just 8.5mm. The PKA and PKC can be easily paralleled for higher power applications and they make ideal components for n+1 parallel redundancy applications.



If your product demands innovative power supplies, yet needs the security of well proven solutions from a reliable source, call Ericsson. And let our technology lead help maintain yours.

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Hong Kong	Ericsson Components AB, Wanchai, Tel: (05) 756 640 Fax: (05) 834 5369
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Italy	Ericsson Components Srl, Milano, Tel: (02) 551 81 597 Fax: (02) 545 97 31
Norway	Ericsson Components A/S, Oslo, Tel: (02) 6 50 190 Fax: (02) 644 138
United States	Ericsson Components Inc, Richardson, TX, Tel: (214) 480 83 00 Fax: (214) 680 10 59
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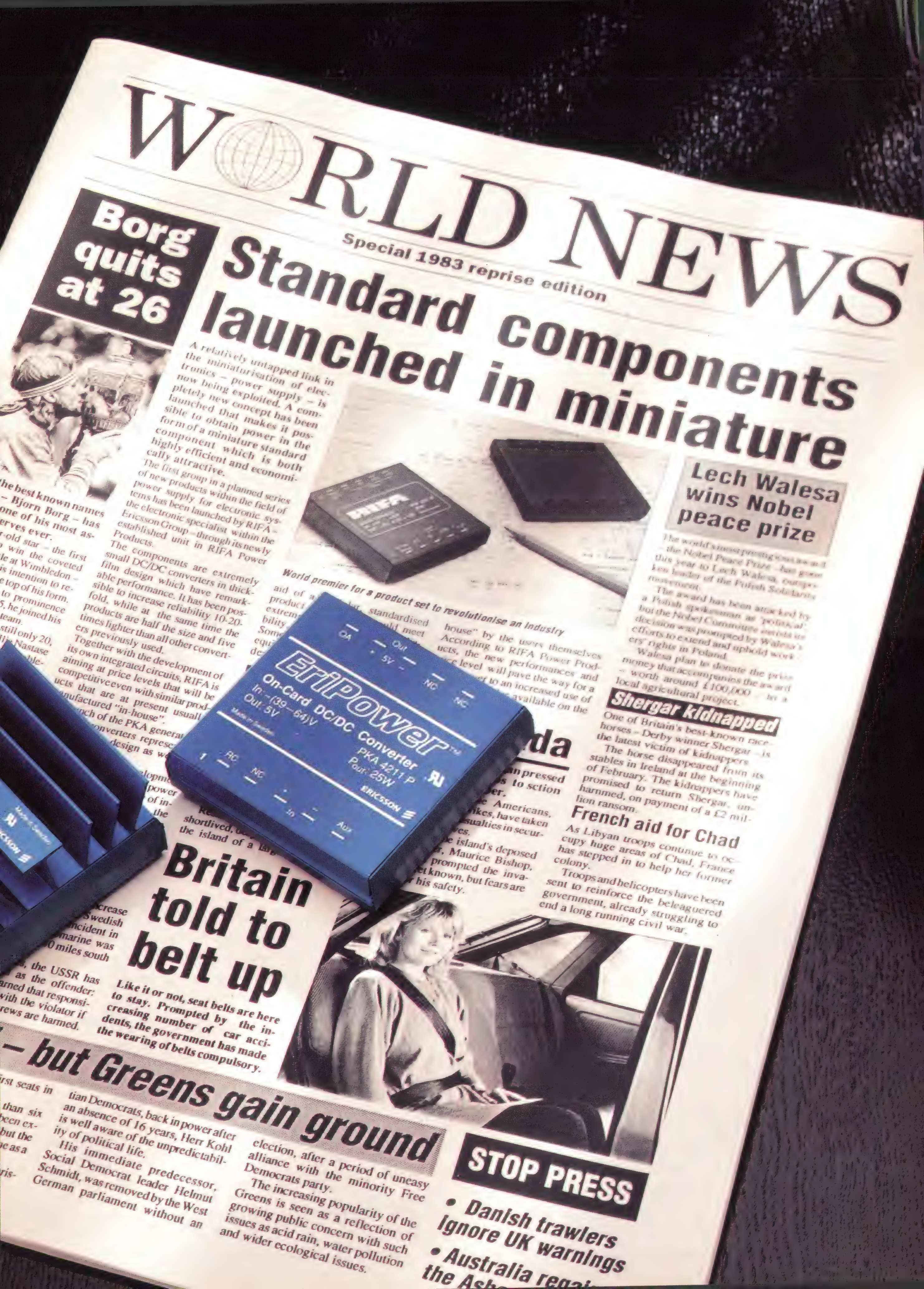

WORLD NEWS

Special 1983 reprise edition

Borg quits at 26

…he best known names – Bjorn Borg – has …one of his most as…erves ever.

…r-old star – the first …o win the coveted …le at Wimbledon – …is intention to re… …e top of his form. …to prominence …5, he joined his …team.

…still only 20, …lie Nastase …ble-

Standard components launched in miniature

A relatively untapped link in the miniaturisation of electronics – power supply – is now being exploited. A completely new concept has been launched that makes it possible to obtain power in the form of a miniature standard component which is both highly efficient and economically attractive.

The first group in a planned series of new products within the field of power supply for electronic systems has been launched by RIFA – the electronic specialist within the Ericsson Group – through its newly established unit in RIFA Power Products.

The components are extremely small DC/DC converters in thick-film design which have remarkable performance. It has been possible to increase reliability 10-20-fold, while at the same time the products are half the size and five times lighter than all other converters previously used.

Together with the development of its own integrated circuits, RIFA is aiming at price levels that will be competitive even with similar products that are at present usuall… …nufactured "in-house". …nch of the PKA general… …onverters represe… …design as w…

…elopm… …power …of in- …the

World premier for a product set to revolutionise an industry

aid of a … standardised product… …uld meet extrem… bility… Som… equi… de…

house" by the users themselves. According to RIFA Power Products, the new performances and …ce level will pave the way for a …er to an increased use of …available on the

Lech Walesa wins Nobel peace prize

The world's most prestigious award – the Nobel Peace Prize – has gone this year to Lech Walesa, outspoken leader of the Polish Solidarity movement.

The award has been attacked by a Polish spokesman as 'political' but the Nobel Committee insists its decision was prompted by Walesa's efforts to extend and uphold workers' rights in Poland.

Walesa plan to donate the prize money that accompanies the award – worth around £100,000 – to a local agricultural project.

Shergar kidnapped

One of Britain's best-known racehorses – Derby winner Shergar – is the latest victim of kidnappers.

The horse disappeared from its stables in Ireland at the beginning of February. The kidnappers have promised to return Shergar, unharmed, on payment of a £2 million ransom.

French aid for Chad

As Libyan troops continue to occupy huge areas of Chad, France has stepped in to help her former colony.

Troops and helicopters have been sent to reinforce the beleaguered government, already struggling to end a long running civil war.

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…e island's deposed …r, Maurice Bishop, … prompted the inva… …et known, but fears are …r his safety.

Re… shortlived, … the island of a larg…

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…, the USSR has … as the offender: …arned that responsi- …with the violator if …rews are harmed.

Britain told to belt up

Like it or not, seat belts are here to stay. Prompted by the increasing number of car accidents, the government has made the wearing of belts compulsory.

… — but Greens gain ground

…irst seats in …

… than six …been ex- …but the …e as a …

…ris- tian Democrats, back in power after an absence of 16 years, Herr Kohl is well aware of the unpredictability of political life.

His immediate predecessor, Social Democrat leader Helmut Schmidt, was removed by the West German parliament without an election, after a period of uneasy alliance with the minority Free Democrats party.

The increasing popularity of the Greens is seen as a reflection of growing public concern with such issues as acid rain, water pollution and wider ecological issues.

STOP PRESS

- **Danish trawlers ignore UK warnings**
- **Australia regai… the Ash…**

NEW PRODUCTS

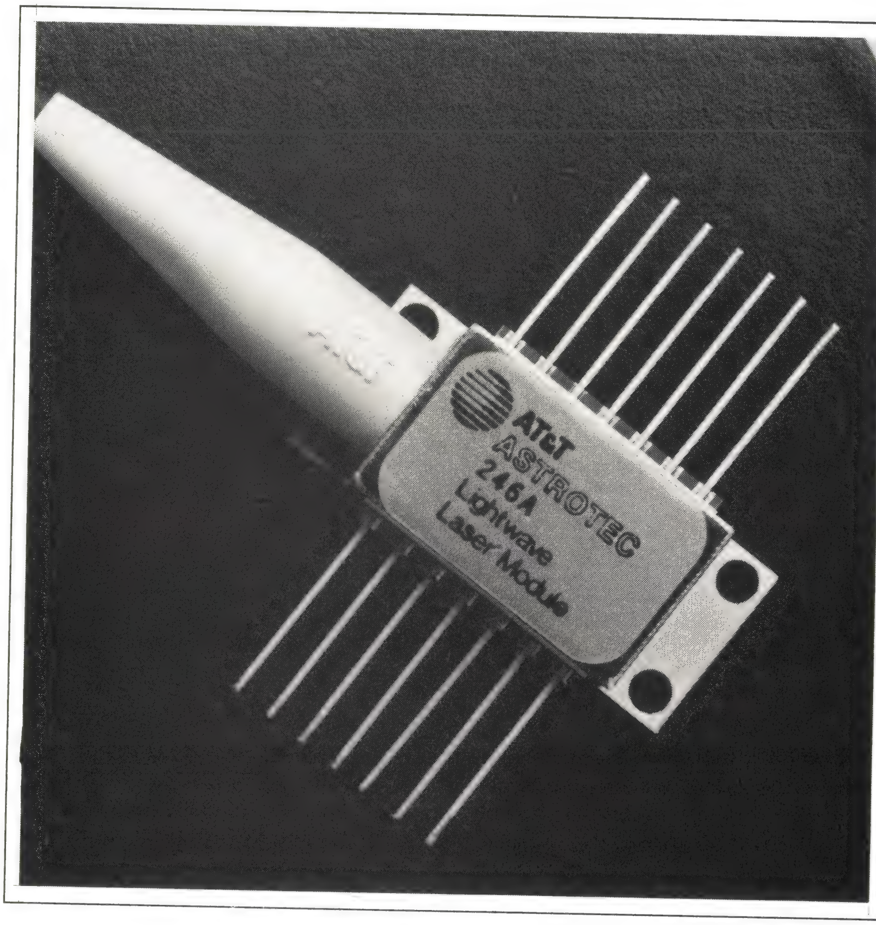
COMPONENTS & POWER SUPPLIES

Isolated Laser Module

- *Outputs 1 dBm*
- *Handles analog or digital transmissions*

The 246-type isolated laser module is available with either a 1.3- or 1.55-μm distributed-feedback laser diode, which handles either analog or digital transmissions. Housed in a 14-pin butterfly, organic-free, hermetic package, the module has a 3-GHz bandwidth and can operate at data rates ranging to 2.5G bps. The module has an average power output of 1 dBm and a minimum optical isolation of 30 dB. In addition to the laser diode, internal isolator, and thermoelectric coolers, the module includes an InGaAs backface PIN (positive intrinsic negative) monitor and temperature sensor. The module will operate over a −40 to +65°C range. $7500. Delivery, eight weeks ARO.

AT&T Microelectronics, Dept 52AL330240, 55 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447. **Circle No. 393**



Sealed Switches

- *Handle 7A loads*
- *Tested in accordance with MIL-STD-202F*

WT Series sealed switches are available in spst, spdt, and double-throw miniature rocker and lever configurations. Contact ratings range from dry circuit to 6A at 125V ac or 7A at 30V dc. The switches are designed to accommodate the rigors of flow or vapor-phase soldering and are 100% tested to MIL-STD-202F, method 112D, test condition D. The units will also withstand 1-minute immersion in cleaning fluids such as water, alcohol, trichloroethene, and mineral spirits. The switches are available with straight, right-angle-horizontal, and right-angle-vertical pc-board terminals. Actuators are available in white, black, and red. $2.50 (1000) for a standard spst model.

American Switch Corp, 134 Water St, Wakefield, MA 01880. Phone (617) 246-1007. FAX (617) 245-4531. **Circle No. 394**

Attenuator Module

- *Limits converter output noise*
- *Has efficiencies ranging to 99%*

The VI-RAM ripple attenuator module accommodates converters with output levels of 5 to 50V and limits total output noise to <3 mV p-p at load levels ranging to 10A. Featuring active and passive filtering capabilities, the unit attenuates both low-frequency input-power-source harmonics and high-frequency switching components in the frequency range of dc to 20 MHz. The module features efficiencies of 93 to 99%, requires no adjustments, and includes remote-sense and output-voltage-trim features. The unit is housed in a package that measures 2.28×2.4×0.5 in. and weighs 2.8 oz. $59.

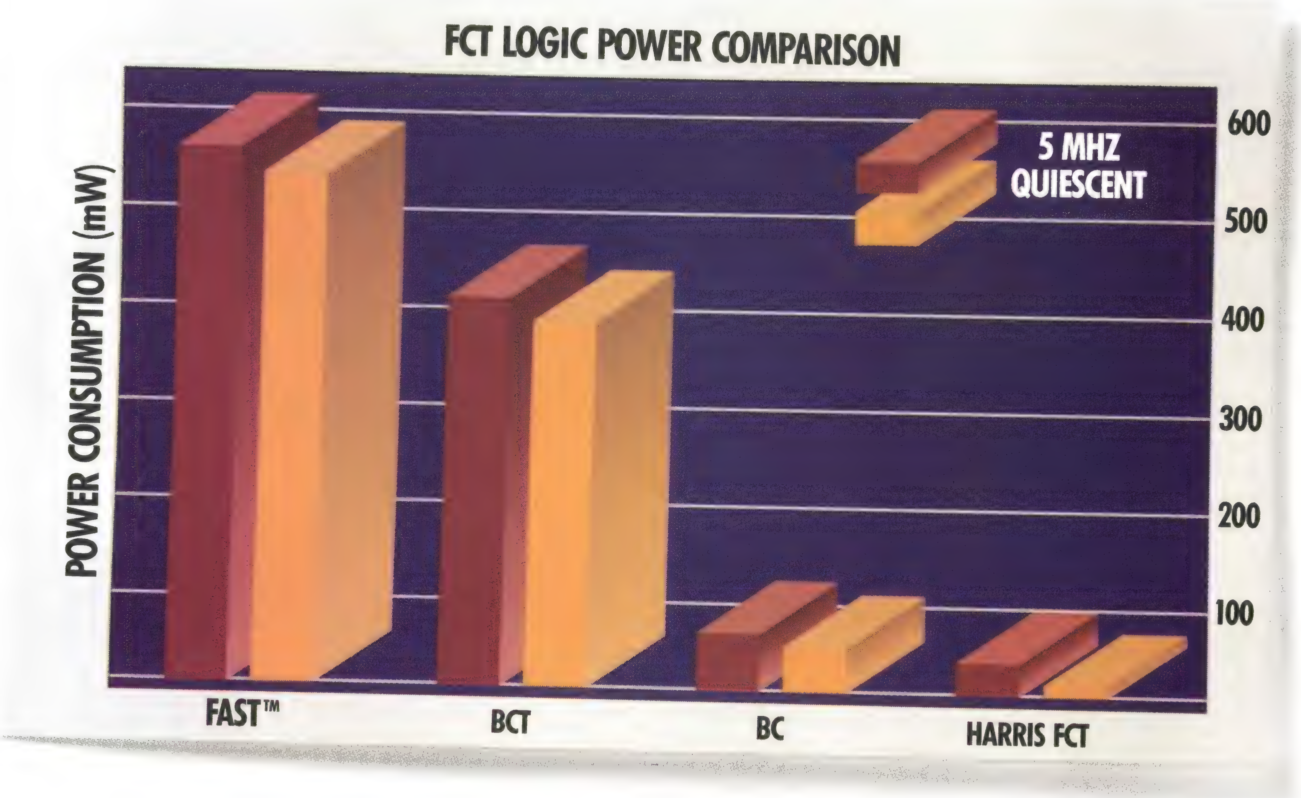
Vicor Corp, 23 Frontage Rd, Andover, MA 01810. Phone (508) 470-2900. FAX (508) 475-6715.
Circle No. 395

Dual LEDs

- *Offer a 90° viewing angle*
- *Accommodate ac applications*

AND170/171 Series dual LEDs are available in red, green, yellow, and orange. Two LEDs are mounted back-to-back in a T-1¾ package to accommodate ac applications. Ver-

We're virtually powerless against the competition.

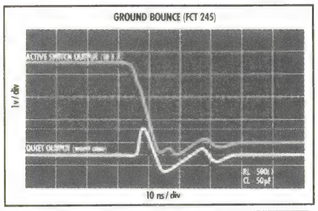


Harris' FCTs Mean High Speed. Not High Power.

When it comes to FCT logic power consumption, less is better. And that's just what Harris' new FCT logic family gives you. Based on our advances in BiCMOS technology, Harris' FCT logic circuits offer you CMOS power consumption at bipolar speeds. With a typical 4.2 nanosecond propagation delay.

Cool Operation.

By reducing power consumption, Harris' FCT logic family generates less heat within your system. Less heat helps increase the reliability of your equipment, along with improving its performance. Noise levels are also lowered, as is ground bounce.



Years of CMOS Innovation.

The new FCT is only the latest advancement in Harris' more powerful, and less power-hungry, CMOS logic.

The new FCT logic family from Harris. Everything you've always wanted in FCT logic. Only less.

For more information on our FCTs, call us at 1-800-4-HARRIS, ext. 1020 (in Canada, 1-800-344-2444, ext. 1020). Or call your local Harris sales office or distributor.

What your vision of the future demands. Today.

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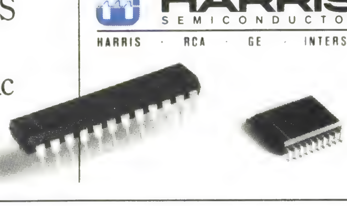
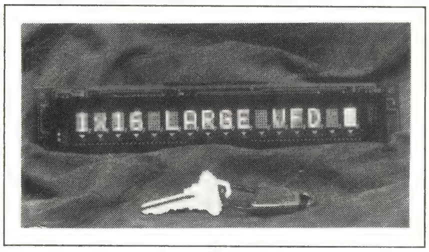


sions are available that feature tinted or diffused lenses with luminous intensities measuring 10 and 6 mcd, respectively. The units operate at forward voltage levels of 2.1V and feature a 90° viewing angle. $0.55 (1000) for the AND170S, a red model.

AND, 770 Airport Blvd, Burlingame, CA 94010. Phone (415) 347-9916. FAX (415) 340-1670.

Circle No. 396



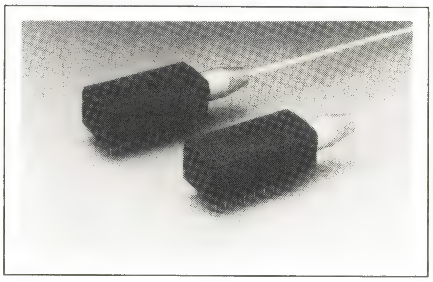
Display Module

- *Is a complete subassembly*
- *Features 200-fL brightness*

Model M16LD03 is a 1-line×16-character vacuum-fluorescent dot-matrix display module. A complete subassembly, the module contains the display, a dc/dc converter, character generator, and refresh circuitry. The unit operates on a single 5V supply and uses a parallel 8-bit ASCII data interface. Measuring 226×50×29 mm, the module displays as many as 239 characters including decimal point and comma. The blue-green display has a brightness rating of 200 fL. Module characters measure 11.25 mm high by 7.2 mm wide. $98 (100).

Futaba Corp of America, Electronic Components Div, 711 E State Pkwy, Schaumburg, IL 60173. Phone (708) 884-1444. FAX (708) 884-1635.

Circle No. 397



Laser-Diode Module

- *Operates at 1300 nm*
- *Outputs as much as 1 mW*

The PLD-1300R laser-diode module operates at 1300 nm. It is housed in a hermetically sealed, TO-type package that contains an InGaAsP laser diode and an integrated InGaAs PIN (positive intrinsic negative) diode, which monitors the laser output. An integral lensing system, which provides very precise positioning and stable alignment over temperature and time, couples the laser output to a single-mode fiber. Optimized, nominal coupled-output level can range from <100 μW to over 1 mW according to customer specifications. The module will operate over a 0 to 60°C range without the need for thermoelectric cooling or heat-sink flanges. The unit is available in two versions—the S model, which comes in a DIP, and the L1, which is available in a TO-FC receptacle package. $526 and $541 for S and L1 versions, respectively.

PCO Inc, 20200 Sunburst St, Chatsworth, CA 91311. Phone (818) 700-1233. FAX (818) 882-7041.

Circle No. 398

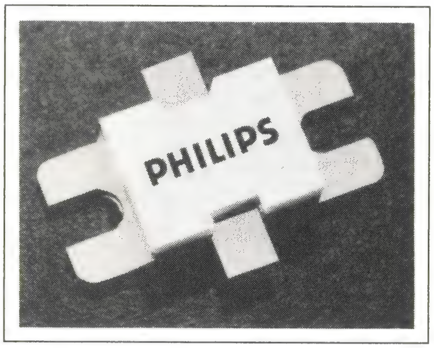
Buffered Enclosure

- *Includes noise filters*
- *Operates from a single supply*

The ALC 1 buffered enclosure consists of an integrated buffer amplifier and any of the company's L or C Series voltage-controlled oscillators (VCOs). The amplifier provides 15-dB-min reverse isolation for the VCO. A pc board maintains proper ground connections between the amp and the VCO to eliminate noise problems. Feed-through capacitors on the power supply and oscillator tuning-input connections filter out noise. A discrete transistor stage isolates power-supply noise from the VCO. Oscillator output is via a capacitively coupled SMA (surface-mount assembly) female connector mounted on the enclosure. The entire assembly is enclosed in an aluminum package measuring 1.8× 1.6× 0.9 in. The module requires a 15V supply. Enclosure, $125; oscillator price depends on the model.

Z-Communications Inc, 5450 NW 33rd Ave, Suite 100, Fort Lauderdale, FL 33309. Phone (305) 735-1000. FAX (305) 735-1094.

Circle No. 399



Microwave Transistor

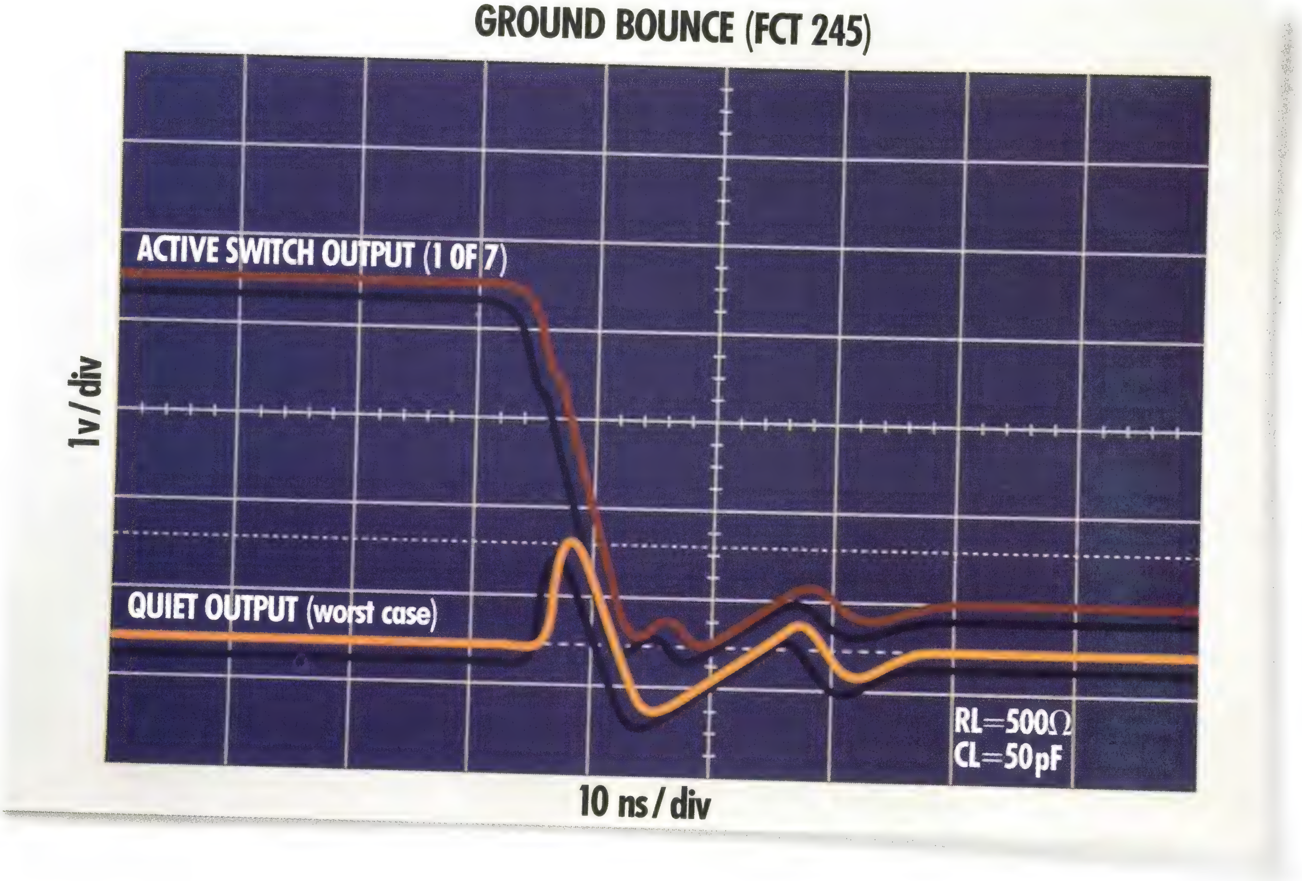
- *Designed for class C operation*
- *Outputs 50W*

Type PXB16050U is an npn, silicon planar epitaxial transistor designed for common-base, class C, narrow-band amplifiers used in satellite links. The unit will output 50W continuous-wave power at 1.6 GHz. Operating from a 28V supply, the transistor has a typical power gain of 9.5 dB and a collector efficiency as high as 52%, The unit contains input and output prematching circuits that facilitate the design of external circuitry and help distribute power equally over the total active area of the transistor. In addition, diffused emitter-ballasting resistors provide accurate current sharing and improve device ruggedness. Gold metallization ensures that device characteristics remain stable over unit lifetime. $240 (1000). Delivery, 10 weeks ARO.

Philips Components, Discrete Products Div, 45 George Washington Hwy, Smithfield, RI 02917. Phone (401) 232-0500.

Circle No. 400

And we're keeping quiet about it.

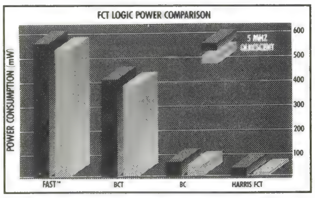


Harris' FCTs Make Less Noise.

Shhhh. Harris' new FCT logic family features low noise plus low power consumption. That's a peaceful thought when you consider that high speed in FCTs used to mean high noise and high chance of error.

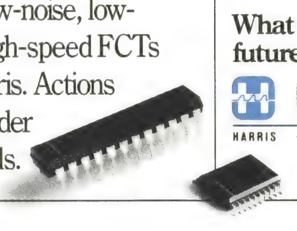
Strong, Silent Type.

By distributing NMOS pulldown technology, Harris is able to limit output voltage swing ($V = 3.7V$ @ $V_{DD} = 5.0V$), lower noise propagation, and still give you the high throughput speeds you need.



Peace Of Mind.

The low-noise, low-power, high-speed FCTs from Harris. Actions speak louder than words.



For more information on our FCTs, call us at 1-800-4-HARRIS, ext. 1020 (in Canada, 1-800-344-2444, ext. 1020). Or call your local Harris sales office or distributor.

What your vision of the future demands. Today.

HARRIS
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Sealed Tuners

- *Meet MIL specs*
- *Tuning scheme involves no disk rotation*

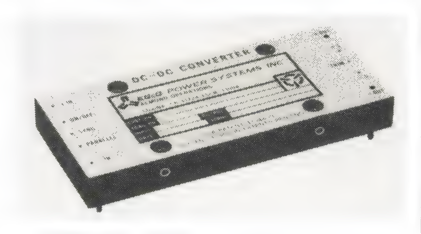
The internal design of these hermetically sealed tuners consists of a disk connected to a bellows. A turn of the external screw moves the disk back and forth within the cavity—there is no disk rotation. This scheme trims the frequency without disturbing the hermetic seal. Three tuner models are available. The V7038 has a 0.125-in.-diameter disk, which travels through 0.035 in. with 3½ turns of the screw. It has a 10-56 threaded outer bushing and is 0.105 in. long. The V7046 and D1A15HS models are housed in quartz cases. The former unit features a 0.07-in.-diameter piston, which has a 0.05-in. travel distance, and the latter model features a 0.15-in.-diameter piston with a 0.16-in. travel distance. All parts meet MIL shock, vibration, and environmental stress requirements. Dielectric constants for the quartz and alumina cases measure 3.8 and 10, respectively. V7038, \$52.50; V7046, \$33.39; D1A15HS, \$14.87 (100).

Voltronics Corp, Box 476, East Hanover, NJ 07936. Phone (201) 887-1517. FAX (201) 887-3349.

Circle No. 401

Militarized DC/DC Converters

- *Deliver 100W output*
- *Offer three outputs*



These military-qualified dc/dc converters accept standard military inputs of 28, 48, 155, and 270V into single, dual, and triple outputs of common dc outputs. They deliver 100W of power and have a conversion efficiency of 77% min for 5V outputs and 80% min for all output levels above 5V. True paralleling capability allows the converters to accommodate N+1 redundancy applications. Key features include remote sensing, paralleling with current sharing, ±5% output-voltage adjust, external sync, and current limiting. Switching frequency equals 100 kHz, and MBTF measures 90,000 hours for a baseplate temperature of 65°C. Operating range spans −55 to +85°C. From \$1600. Delivery, stock to 16 weeks ARO.

EG&G Power Systems, 1330 E Cypress St, Covina, CA 91724. Phone (818) 967-9521. FAX (818) 967-3151.

Circle No. 402

When your resistor doesn't act like a resistor… call Carborundum

Carborundum® noninductive bulk ceramic resistors solve tough resistance problems, save money and space.

Today's requirements for higher voltages, energies and frequencies in radar, communications, pulse power systems and other high-energy applications may exceed the capability of conventional resistors. The solution: Specify Carborundum® ceramic power resistors to solve tough problems.

Regardless of the pulse shape, we have the resistor. Our type AS can absorb huge amounts of energy in millisecond pulses; type A solves high-resistance problems in high-voltage situations; type SP handles large amounts of power from 60 cycles through VHF.

Type	Key Features	Application Areas
AS	Noninductive High voltage/energy	Capacitor crowbar circuits Pulse-forming networks Impulse voltage generators High-voltage snubber circuits
A	Noninductive High resistance	Grounding resistors Voltage dividers
SP	Noninductive High power	High-power/frequency loads Parasitic suppression Current limiting snubber circuits

Some customers come to us after no one else can do the job. It makes sense to *start* with us.

For more information on ceramic power resistors and our line of thermistors and varistors, call or write today.

The Carborundum Company
Electric Products Division
P.O. Box 664
Niagara Falls, New York 14302
Telephone 716 278-2521
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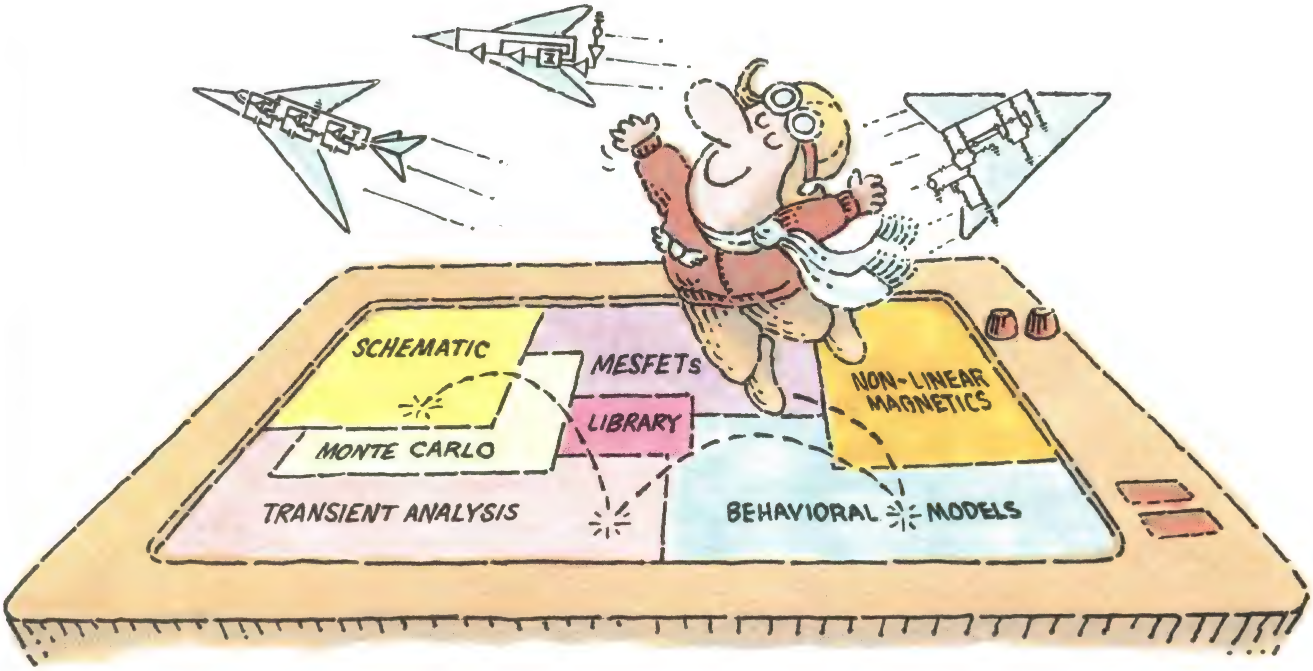
CARBORUNDUM

CIRCLE NO. 17



THE NEW MICRO-CAP III™. SO YOU CAN TEST-FLY EVEN MORE MODELS.

It wasn't easy. But we did it. Made the long-time best-selling IBM® PC-based interactive CAE tool even better.

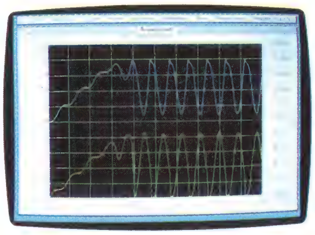
Take modeling power. We've significantly expanded math expression capabilities to permit comprehensive analog behavioral modeling. And, beyond Gummel Poon BJT and Level 3 MOS, you're now ready for nonlinear magnetics modeling. Even MESFET modeling.

Analysis and simulation is faster, too. Because the program's now in "C" and assembly language. That also means more capacity—for simulating even larger circuits.

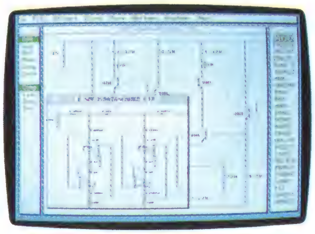
As always, count on fast circuit creation, thanks to window-based operation and a schematic editor. Rapid, right-from-schematics analysis—AC, DC, fourier and transient—via SPICE-like routines. The ability to combine digital/analog circuit simulations using integrated switch models and parameterized macros. And stepped component values that streamline multiple-plot generation.

And don't forget MICRO-CAP III's extended routine list—from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

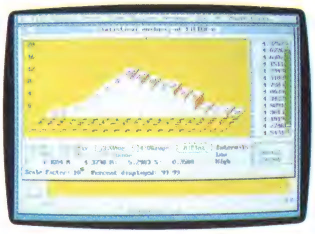
Cost? Still only $1495. Evaluation versions still only $150. Brochure and demo disk still free for the asking. Call or write for yours today. And see how easily you can get ideas up and flying.



Transient analysis



Schematic editor



Monte Carlo analysis

spectrum

1021 S. Wolfe Road
Sunnyvale, CA 94086
(408) 738-4387

CIRCLE NO. 131

NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

FPGA Development System

- *Captures and simulates an FPGA circuit*
- *Can drive an FPGA programmer*

The TI Action Logic System (TI-ALS) is an FPGA-development (field programmable gate array) system that consists of both software and programming hardware. You can capture schematics, simulate and verify their operation, and perform placement and routing as well as timing analysis. The program is menu-driven to make it easy for users who are not familiar with gate-array-design methods. The program works with existing schematic-capture software and the vendor's TPC Series Macro library; this library consists of 212 of the most frequently used logic-consolidation macros. After you've completed the circuit-design processes on the host computer, you can export the files to the TI-ALS for design verification, automatic placement and routing, and timing analysis. Pricing depends on the host computer and the capture software. Starter system for Orcad capture- and simulation-system for 80386-based PCs, $7950; with the vendor's Activator programmer, $9950.

Texas Instruments Inc, Semiconductor Group (SC-9002), Box 809066, Dallas, TX 75380. Phone (800) 232-3200 ext 700.

Circle No. 357

Extender For Multiuser DOS Environment

- *Runs under Theos operating system*
- *Allows several users to share a DOS application program*

The Theo+DOS Version 1.1 software package runs on 80386-based PCs under the Theos operating system. The package allows multiple users to run the same DOS application program simultaneously and to exchange files. Each user can also run a combination of DOS programs and multiuser Theos programs written for a specific application. To add users, you just connect an inexpensive terminal to a multiport serial board that plugs into an expansion slot of your PC. Theo+DOS executes programs under an actual copy of PC-DOS or MS-DOS, thereby guaranteeing that the application will be compatible with the computer. A special memory-management feature allows users to access 30% more memory than the standard 640k bytes. The extender also works with VGA, EGA, CGA, and Hercules graphics boards. Any user can switch between as many as 12 active DOS or Theos applications by simply pressing a hot key associated with a particular application program. $999 for a 9-user license.

Theos Software Corp, 1777 Botelho Dr, Suite 360, Walnut Creek, CA 94596. Phone (415) 935-1118. FAX (415) 935-1177.

Circle No. 358

Universal Cross-Assembler

- *Table-driven*
- *Assembles source code for more than 20 different μPs*

Cross-16 version 2.0 is a table-driven cross-assembler that lets you assemble source code for more than 20 different μPs, using the chip manufacturer's original assembly-language mnemonics. The cross-assembler allows you to use arithmetic operators and integer constants that are identical in form and precedence to those used by ANSI C, as well as several common assembler conventions. The cross-assembler reads the assembly-language source file and a corresponding table of assembly-language instructions; it generates a list file and an absolute object file in binary, Motorola, or Intel Hex format. You can download the object file to most EPROM programmers, EPROM emulators, and in-circuit emulators. The package comes with tables for the instruction sets of chip families from Motorola, Intel, National Semiconductor, and Zilog; the user's manual contains instructions for writing new processor tables and modifying those that come with the package. To run Cross-16, you'll need an IBM PC or compatible that has at least 256k bytes of RAM and

The Complete Electronic Design Solution.

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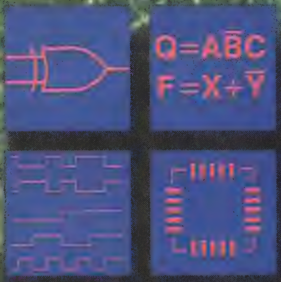
Tango is the pacesetter in affordable, PC-based electronic design. It offers the quality and performance engineering professionals demand, and the easiest-to-use interface available on any platform, at any price.



Tango's powerful lineup. Build your personal CAE/CAD workstation with Tango's start-to-finish design tools. **Tango-Schematic**,™ just $495, includes over 8,000 SEDCO™ parts, the largest library on the PC. Experience **Tango-PLD**'s powerful top-down approach to logic design for only $495. Add interactive logic simulation for up to 40,000 gates with **Susie**.™

Starting at just $595, our popular PCB layout tools have designed *tens of thousands* of boards. There's **Tango-PCB PLUS**,™ for complex designs and **Tango-PCB**,™ a comprehensive, yet economical program for less demanding requirements. Tango designers have three fast and efficient autorouting options: the high-performance **Tango-Route**;™ multi-grid, multi-layer **Tango-Route PLUS**;™ and **Superoute**,™ the industry-leading rip-up and re-try, 100% completion autorouter. Finally, there's the **SMT Plus Library**™ supplying proven land patterns for sophisticated SMT designs.

Tango extras at no extra charge. Your investment in Tango software includes clear, concise documentation; responsive technical support, free by phone or fax; first year of updates free, with affordable annual renewals; our 24-hour Tango BBS; directories of service bureaus and design consultants; a quarterly newsletter; and our money-back guarantee. Give us a call to discuss your design requirements. You'll find our customer service is as friendly as our software.

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CIRCLE NO. 132

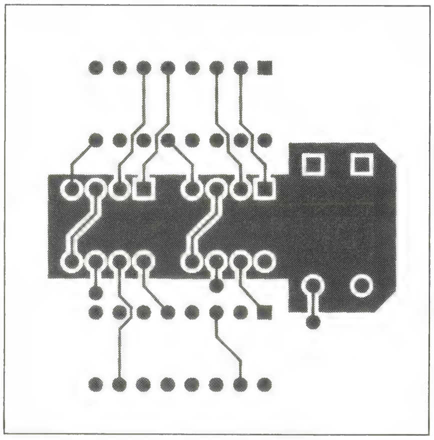
runs under DOS 2.0 or a later version. $99. Purchasers of earlier versions may upgrade to version 2.0 at half-price.

Universal Cross Assemblers, Box 6158, Saint John, NB Canada E2L 4R6. Phone and FAX (506) 847-0681. **Circle No. 359**

Built-In Analog Ground Plane For CAE Software

- *Ground-plane feature automatically clears pad space*
- *Can create arbitrarily shaped copper areas*

An enhanced version of DC/CAD software uses artificial-intelligence techniques to facilitate the creation of ground-plane areas on a circuit board. The ground-plane feature automatically puts clearance around pads and routes that reside inside copper-plane areas, and attaches the common plane to the copper net with a thermal relief. To change the circuitry within the copper area, just make the changes to the routes and instruct the editor to recalculate the copper plane. The basic software package runs on IBM PCs, PS/2s, and compatibles. $495.

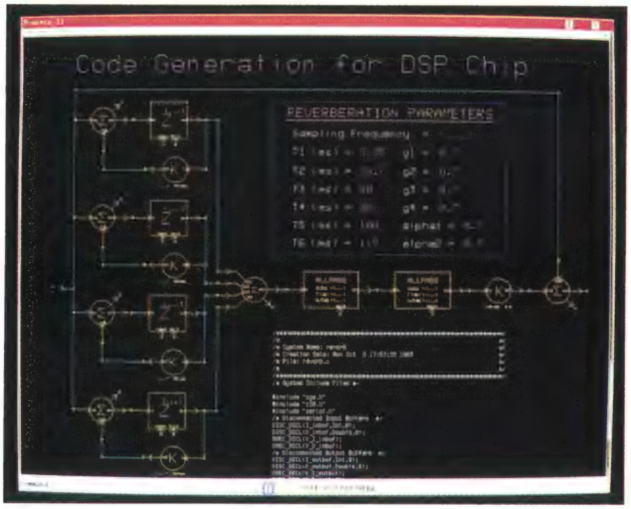


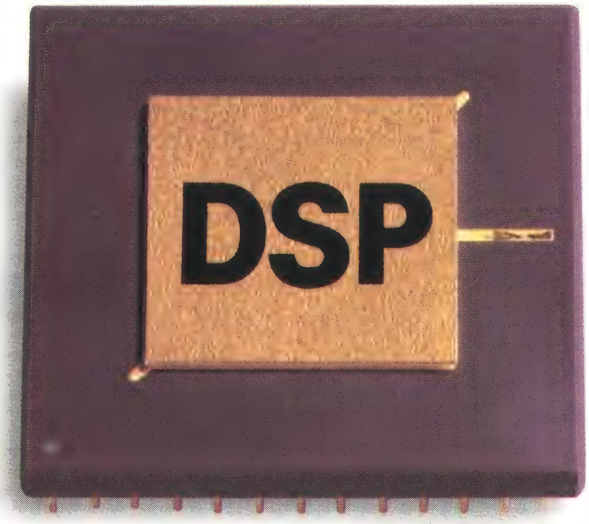
Design Computation Inc, Sherman Square, Rte 33, Farmingdale, NJ 07727. Phone (201) 938-6661. **Circle No. 360**

CASE for IBM RISC Systems

- *Provides repository and services to link CASE tools*
- *Has tools to help in managing all phases of software development*

The Integrated Project Support Environment (IPSE) consists of two complementary suites of tools: the Software Backplane, which is a framework that provides a repository and services for linking disparate CASE tools, data, and methodologies; and the SoftBoard Series, which is a set of applications that assist in the development and management of all phases of a project from requirements definition to testing of the code. These tools currently run on IBM's RT PC and will be available for IBM's RISC System/6000 family of workstations as soon as the company begins shipping them. Single workstation: Software Backplane, $4950; Inte-





GO FROM IDEA. TO PROTOTYPE.

gration SoftBoard, $7950; Project SoftBoard, $2250.

Atherton Technology, 1333 Bordeaux Dr, Sunnyvale, CA 94089. Phone (408) 734-9822.
Circle No. 361

Critical Path Analyzer

- *Calculates critical paths*
- *Works with discrete logic, gate arrays, and standard cells*

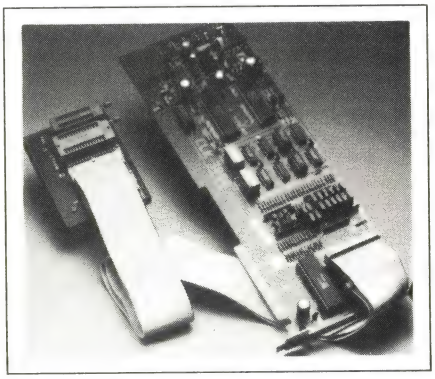
Quilpath analyzes digital circuits, taking into account loading effects, wiring delays, differences in rising- and falling-edge speeds, and inverting and noninverting paths. The program automatically calculates the maximum or minimum path through a circuit. You can make the program perform a global analysis of the complete circuit, or you can focus the analysis on selected paths. The program runs on IBM PCs and compatibles, and is menu-driven. By means of an EDIF (Electronic Data Interchange Format) translator, the program can accept input from most popular schematic-capture packages. You can download a demo version (at no charge) from the vendor's 2400-bps bulletin-board system (BBS). $200.

Quilted Logic Technology Inc, 204 N El Camino Real, Suite E512, Encinitas, CA 92024. Phone (619) 489-1726. BBS (619) 632-0718.
Circle No. 362

EPROM Programmer

- *Plugs into your PC*
- *Four 1M-bit EPROM programming capacity*

The CLK-6100 is an EPROM programmer on a plug-in card to suit IBM PC/XTs, PC/ATs, and compatibles. A range of EPROM adapters connects by ribbon cable to provide a maximum programming capacity of 12 256k-bit or four 1M-bit EPROMs. The device comes with support software for programming all 27xx-series EPROMs and 87xx microcontrollers. CLK-6100A with one adapter, £99.



Flight Electronics Ltd, Flight House, Ascupart St, Southampton SO1 1LU, UK. Phone (703) 227721. FAX (703) 330039. **Circle No. 363**

AUTOMATICALLY.

The Code Generation System of the Signal Processing WorkSystem™ automatically converts a DSP or communications system design into stand-alone C. This can then be targeted to a variety of DSP microprocessors to create instant prototypes. SPW™ also produces fully-documented C code to run on other platforms.

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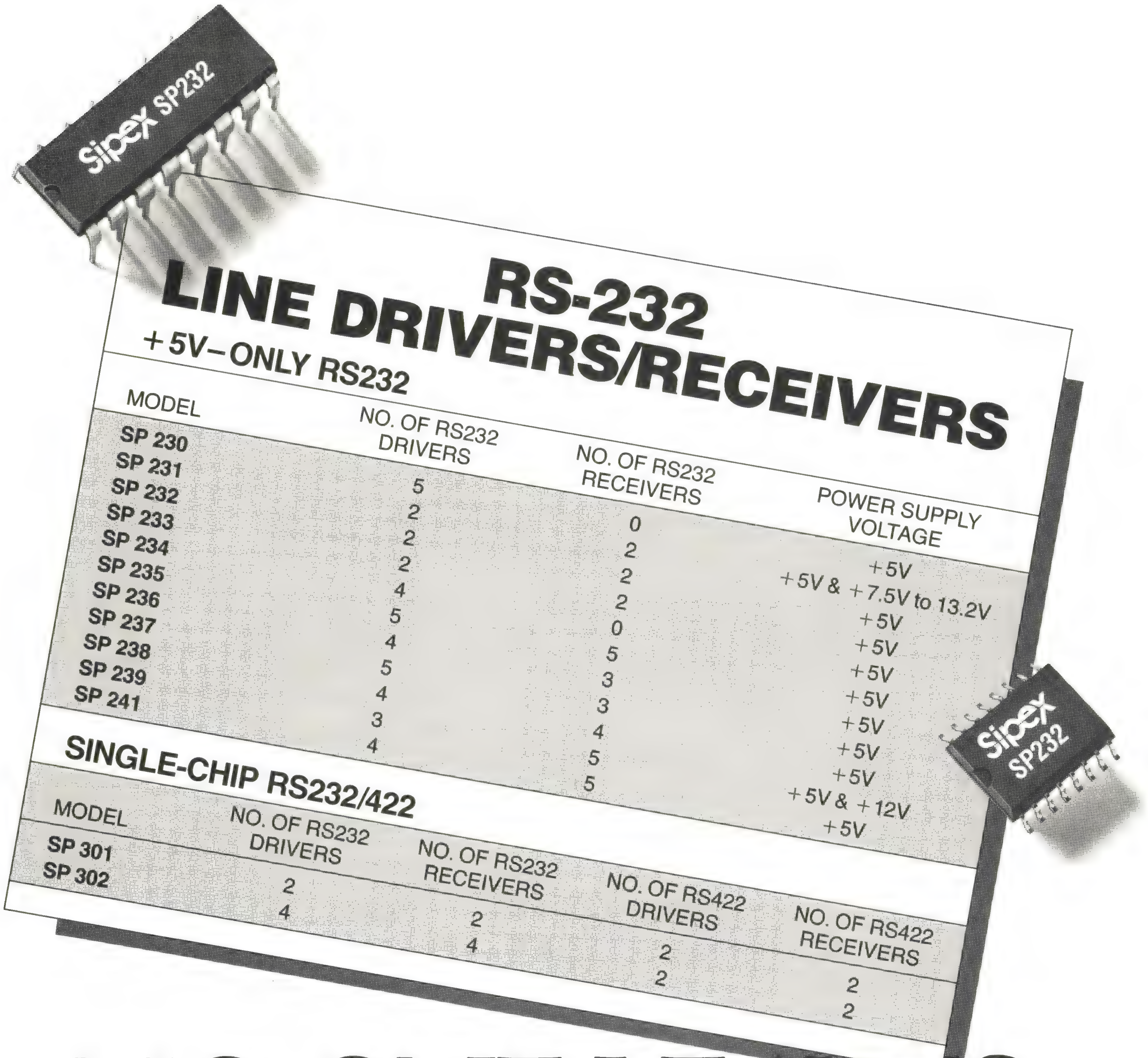

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SP 235	5	5	+5V
SP 236	4	3	+5V
SP 237	5	3	+5V
SP 238	4	4	+5V
SP 239	3	5	+5V & +12V
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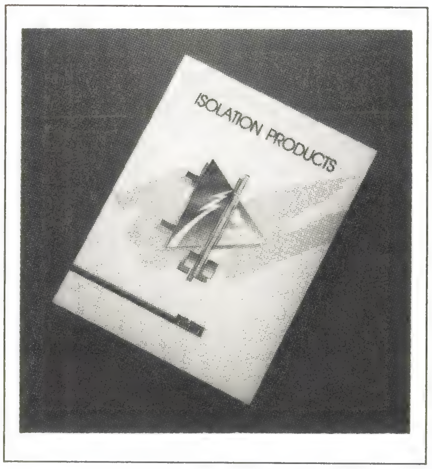
LITERATURE



Listing Of Analog Isolation Products

The company's guide, *Isolation Products*, presents specifications for more than 20 isolations, including isolated signal amplifiers, dc/dc power supplies, and signal and power-supply combinations. The publication details products with a broad range of isolation ratings from 750 to 3500V rms; with transformer, optical, and capacitive barrier technologies; and packaged in plastic DIPs, surface-mount SOICs, and hermetically sealed ceramic DIPs. Some new products include the ISO212 signal/power combination in a ZIP (zig-zag in-line package); the ISO122P, a small signal-isolation amplifier; and the ISO102/ISO106 signal amps with rated isolation to 3500V rms. The applications section discusses ECG (electrocardiogram) amplification; ac power measurement, isolated integrating A/D conversion, and isolated current-loop driver output for industrial control.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. **Circle No. 351**

Publication Describes Integrated CAD System

The vendor's trifold brochure discusses the functions and features of EE Designer III/Extended Version 2.2. The pamphlet explains how the integrated configuration of the software makes it easier to learn than other versions. In addition to discussing the software's functions, color photos illustrate how the software handles diverse design tasks such as schematic capture, A/D simulation, thermal analysis, pc-board layout, autorouting, and fabrication drawings. Finally, the brochure offers a complete list of specifications, interfaces to other software systems, and basic hardware requirements for running the software.

Visionics Corp, 3032 Bunker Hill Lane, Suite 201, Santa Clara, CA 95054. **Circle No. 352**

Release Of Development-Tool Guide

The company's *Development Tool Guide* provides a catalog of emulators and applications information. An application note, in discussing the use of source-level debuggers, points out the improvements in this technology, especially when working in C. The note also deals with the subtle compatibility issues that arise when using a source-level debugger. According to the vendor, the guide is the only complete catalog of emulators.

Softaid Inc, 8930 Route 108, Columbia, MD 21045. **Circle No. 353**

Product-Family Handbooks

The company's set of 10 handbooks consists of the following titles: *Peripherals*, $24.95; *Memory*, $19.95; *Microcomputer Boards and Systems*, $19.95; *Microcommunications*, (two volumes) $26.95; *16-Bit Embedded Controllers*, $20; *8-Bit Embedded Controllers*, $20; *16/32-Bit Embedded Processors*, $21.95; *Embedded Applications*, $20; *Programmable Logic*, $18; and *Microprocessors*, $24.95. The Product Guide is free. You can purchase the publications individually, or as a set for $159.

Intel Literature Sales, Box 58130, Santa Clara, CA 95052. **INQUIRE DIRECT**

Computer-Based Interfaces Presented

The vendor's 1990 Volume 22 Catalog presents data on complete lines of data-acquisition, industrial-control and monitoring, video-imaging, signal-conditioning, personal-instrumentation, and communications products for IBM PC, PC/XT, PC/AT, PS/2, and Macintosh II microcomputers and compatibles. Some of the products featured in the 384-pg publication are WorkHorse, a series of high-speed industrial-control and monitoring products; the DAS-HRES, a 16-bit data-acquisition board; and the MV-Spectrum, a VGA graphics/overlay frame-grabber board. The handbook also contains selection guides and application notes.

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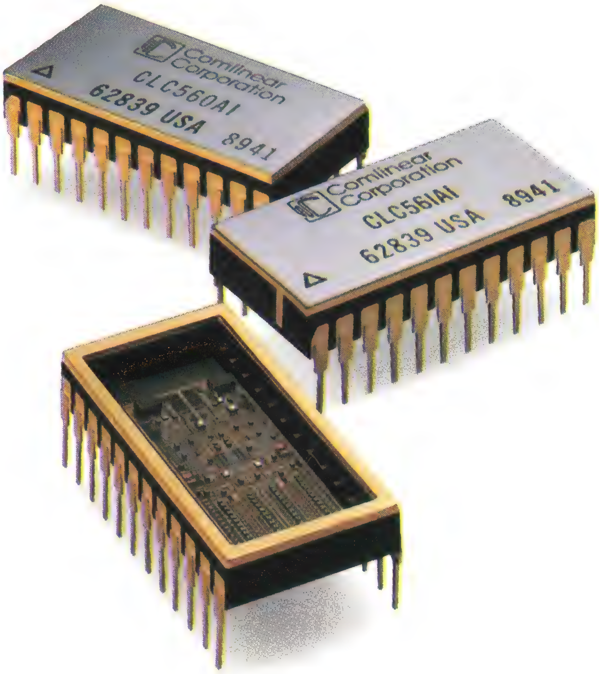

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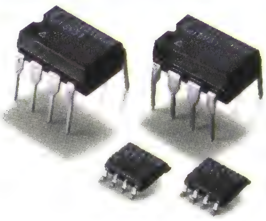

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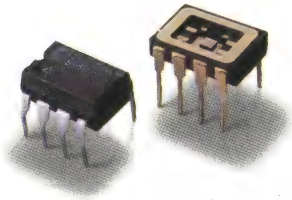

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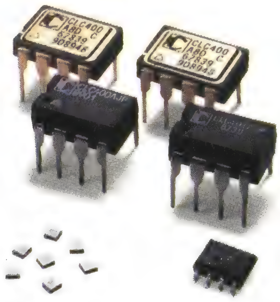

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LITERATURE

Fiber-Optic Routes For Long-Haul Carriers Mapped

The company's fifth edition of its fiber-optic long-haul-systems map illustrates the routes of 19 long-distance telephone companies located in the US and Canada. The map features routes in operation as well as routes planned for 300 cities in 1990. Also included are changes wrought by mergers and acquisitions during the past year. The map measures 29½×22 in. $75.

KMI, America's Cup Ave at 31 Bridge St, Newport, RI 02840.

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Library Of Spice Macromodel Op Amps

This IBM PC/AT-compatible disk offers more than 40 Spice macromodels for the company's op amps. Also included on the disk is a demonstration version of PSpice from MicroSim Corp, which allows you to test models in many standard configurations.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

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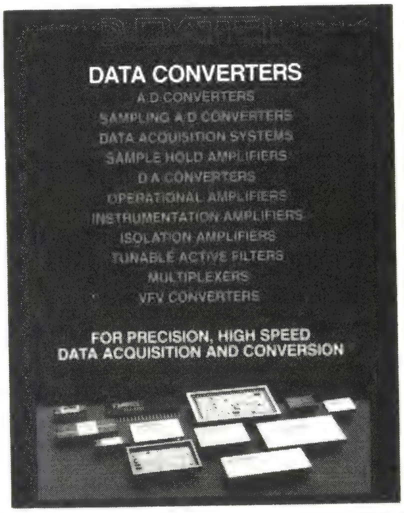

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This 6-pg foldout brochure lists data-converter components and highlights more than 25 new prod-

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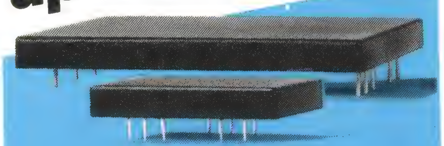

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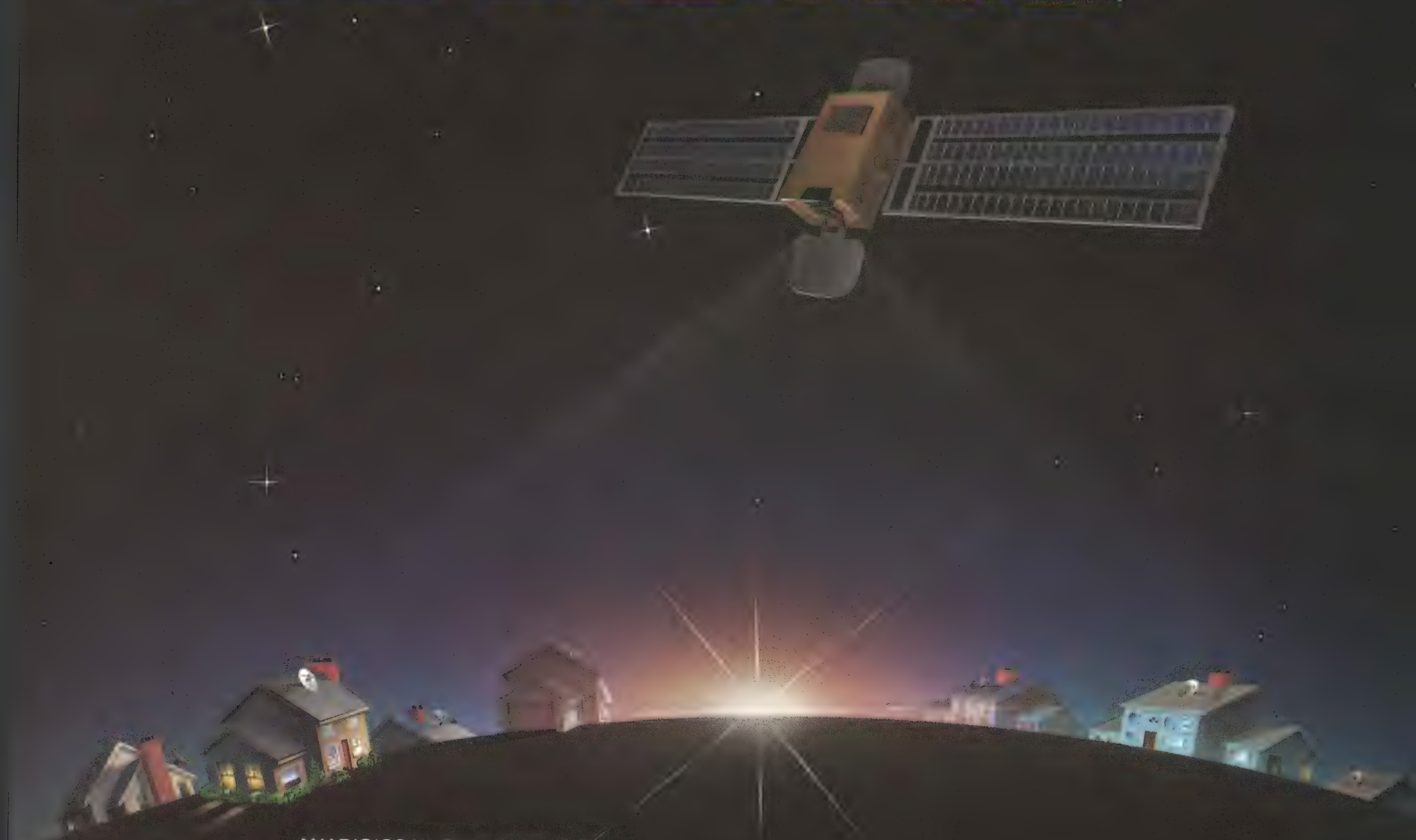
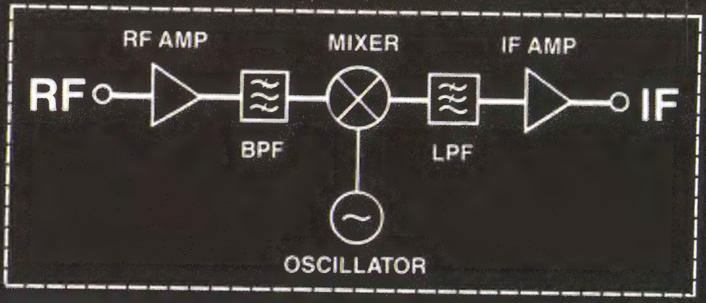


ANADIGICS Ku-Band GaAs IC Chip



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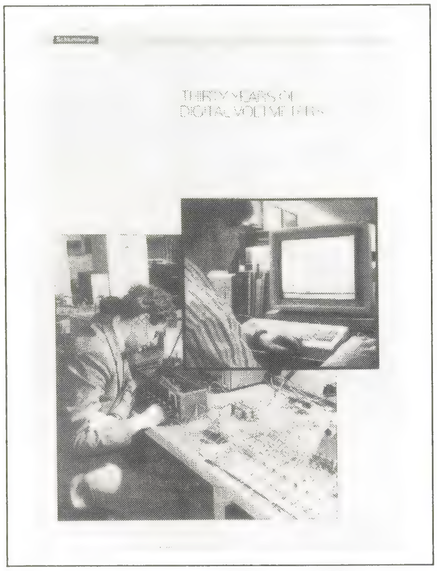
Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. **Circle No. 355**



30-Year Evolution Of Digital Voltmeter

This 12-pg brochure traces digital voltmeter development since 1960. Liberally illustrated, the publication compares specifications of models introduced during the period. It examines principles of operation and key component technologies, notably for displays and internal reference standards, and it reviews calibration and traceability figures over the years.

Schlumberger Technologies, Instruments Div, Victoria Rd, Farnborough GU14 7PW, UK.

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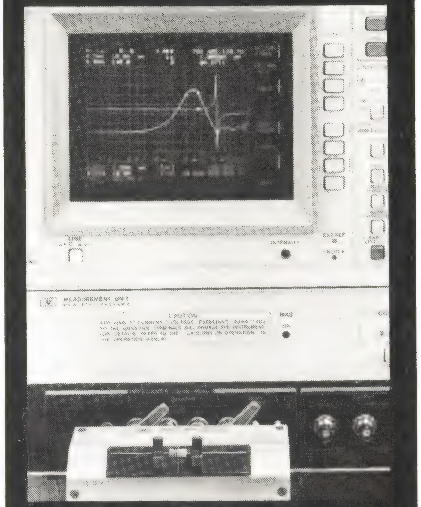

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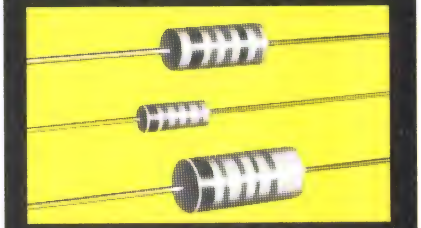

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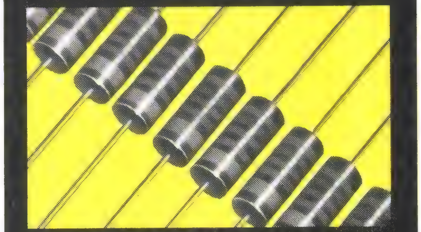

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EDN covers new and developing technologies to inform its readers of practical design matters that will be of concern to them at once or in the near future.

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Peter D Coley
VP/Publisher
Newton, MA 02158
(617) 964-3030; Telex 940573
Ora Dunbar, Assistant/Sales Coordinator

Mark J Holdreith
Associate Publisher
Newton, MA 02158
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Heather McElkenny, Assistant

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NEW ENGLAND
Chris Platt, Regional Manager
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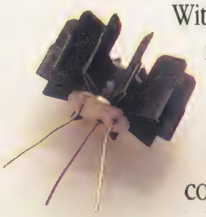

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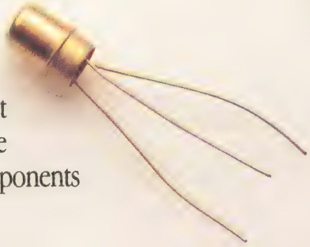

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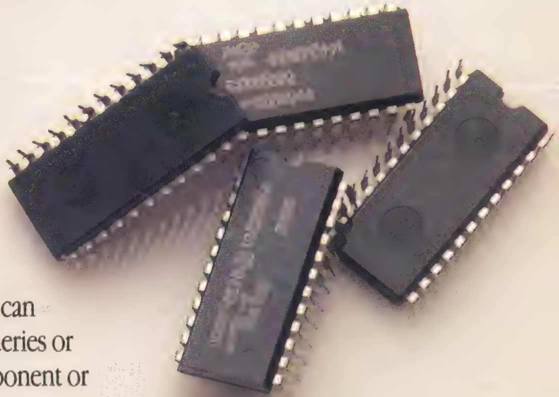

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Treat yourself to a spy thriller

The Cuckoo's Egg, by Clifford Stoll. 326 pgs; $19.95. ISBN 0-385-24946-2. Doubleday, New York, NY 1989.

Here's a detective story that most EDN readers will enjoy—at least those with an interest in international sleuthing, computers, and hackers. Many nontechnical readers will enjoy it, too. The story is even more exciting, because what you read about actually happened to the author. In the tradition of Alistair McLean and Tom Clancy, Stoll spins out a story of espionage and computer hacking that will hold your attention until you finish the book. A word to the wise—don't start this book on a weeknight unless you're a speed reader.

Like most mysteries, Stoll's starts with a small clue: a 75-cent accounting error for computer time at the Lawrence Berkeley Laboratory (LBL) where he works. Tracking down such a small error seems like a good first job for an astronomer who now finds himself transplanted to LBL's computer center. At first, finding the error looks easy because several programs have kept track of computer use, and the accounting information should be the same for each. But for Stoll, the Unix-based computers are unknown territory, so it takes him several days to realize that the accounts are accurate. Instead, an unauthorized user has stolen the unaccounted-for time.

But how do you track down such a person? Stoll starts by attaching a printer to each incoming serial line so that he'll have a hard copy of every computer access—including log-ons, file transfers, and program dumps. A computer program within the system could do the same things, but Stoll reasons that a proficient hacker might recognize the presence of such a program and stay away from the computer, thus foiling attempts to trace him. Stoll's intuition about the hacker pays off—he turns out to know the computer's Unix operating system well and gains access to it by laying a "cuckoo's egg" in the system.

Like the cuckoo bird that slips its eggs into other birds' nests, the hacker places his "egg" within Unix so that he becomes a super user—one who can control the entire computer system. Even when you know how a hacker gets into your computer, tracking him down can involve months of careful sleuthing: tracing phone lines and working with other computer-systems people around the US, and with telephone service people. Stoll does it all, both on his own and with others.

Although Stoll's hacker damages no files or programs, the topics he seeks involve military research and include topics such as the Strategic Defense Initiative (SDI), Strategic Air Command (SAC), and White Sands Missile Range. Also, once the hacker gets into the LBL computer, he probes hundreds of other computers through the US Defense Department's Milnet and Arpanet. To Stoll, searches for key words and acronyms such as SDI on Arpanet are signs of danger. This hacker is looking for serious information. It is unlikely he's a high-school kid with a PC and a new modem, or a college student using a terminal on the University of California's Berkeley campus.

Now that Stoll's printer outputs list such information searches, it should be easy to interest the FBI, CIA, or National Security Agency (NSA) in the attempted break-ins. One of Stoll's key points is that these government agencies—and others—get involved reluctantly and hesitate to take action unless they involve outright theft or loss of assets. Stoll's persistence eventually persuades these groups that he is serious and that the hacker is a threat. In fact, Stoll devotes quite a bit of the book to the details of "working" with the government.

Stoll's experiences reinforce my pessimistic view of what the US government is doing—if anything—to protect and secure computer systems and information from unauthorized users. All too often the protectors of the computers that Stoll notes in his book swear that their systems are immune to attack. Stoll's traces and printouts prove otherwise, and he makes the point that if your computer has a line that's available to outsiders, it's open to attack. Stoll's unflattering portrait of the government agencies begs for a response and for decisive action. Too many users have little concern for computer security.

In all fairness, many of the people that Stoll worked with cooperated to the extent they could, as individuals, and worked to keep Stoll on the hacker's trail. But I won't spoil the chase and the ending for you. If you're interested in a good technical thriller that will hold your interest and make you think about the security of your own computers, this is the book for you.—***Jon Titus***

WHAT'S COMING IN EDN

EDN Magazine's April 26, 1990, issue will feature a staff-written Special Report on DSP add-in boards for IBM PCs. Part 1 of our designer's guide to precision current sources will discuss current-source basics and analyze practical circuits. EDN's All-Star PC project will continue with part 4, which will focus on operating-system software. Also, remember to look for our regular departments.

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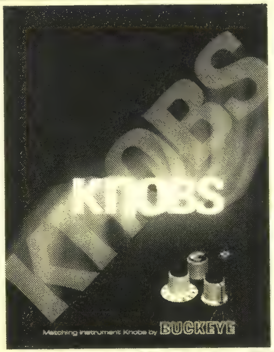

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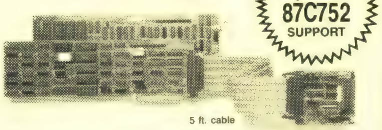

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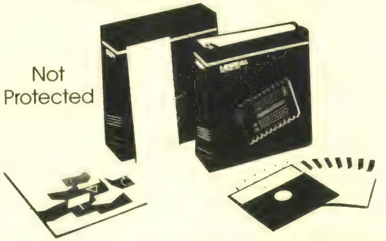

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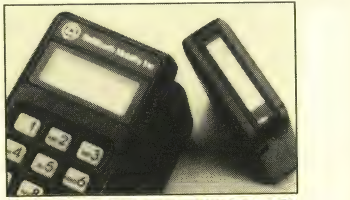

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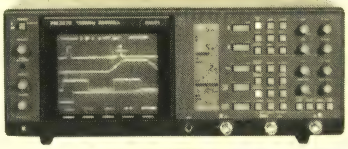

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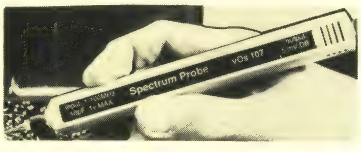

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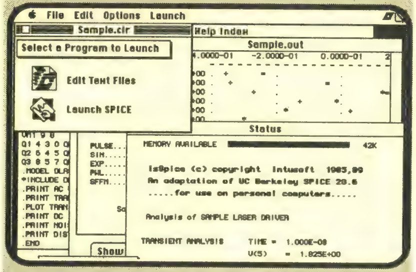

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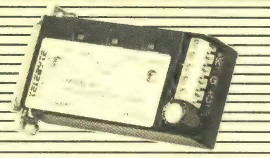

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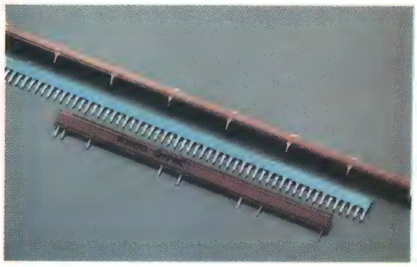

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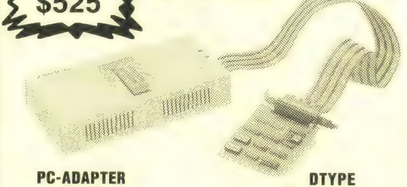

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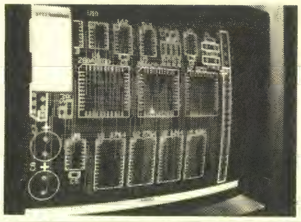

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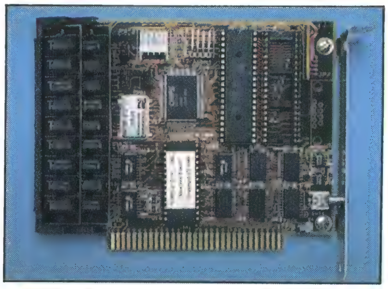

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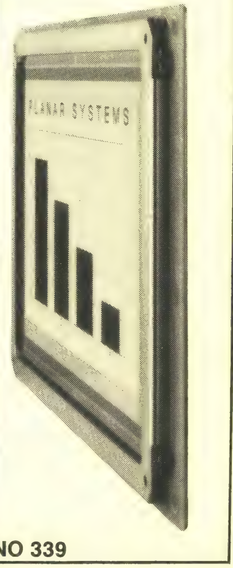

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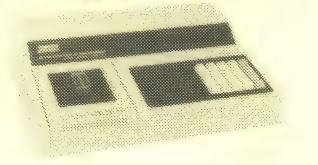

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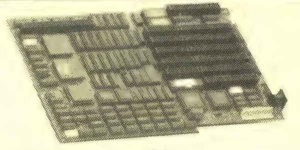

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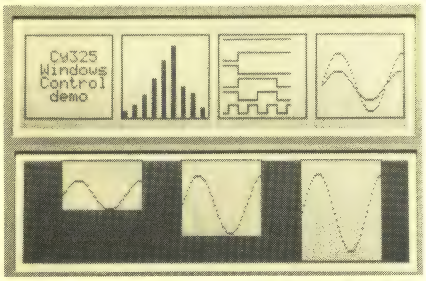

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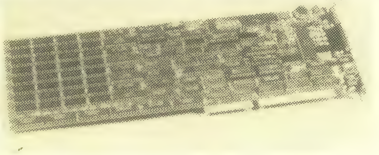

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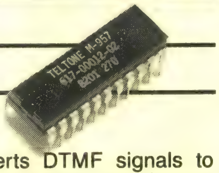

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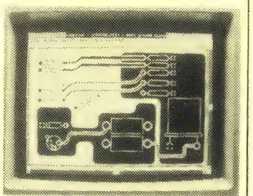

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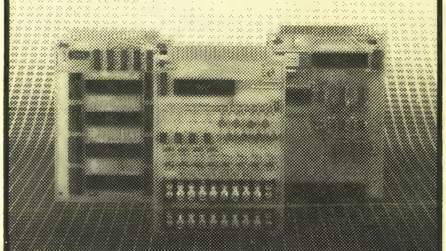

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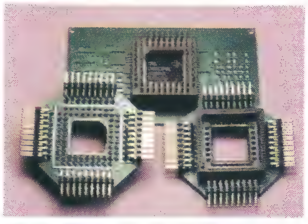

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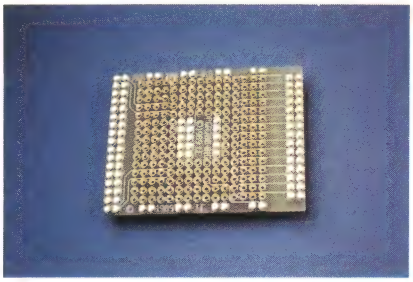

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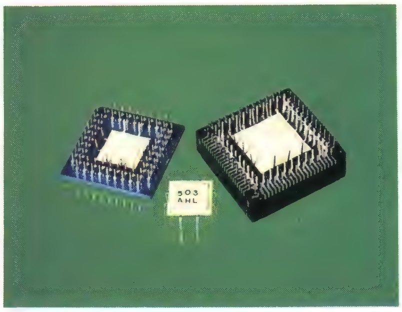

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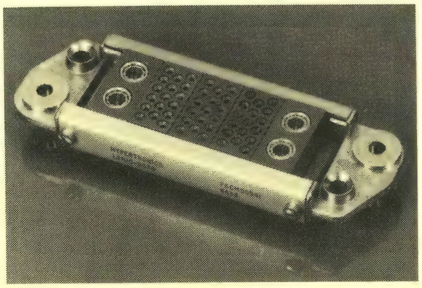

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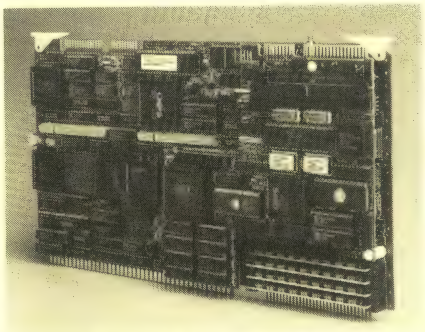

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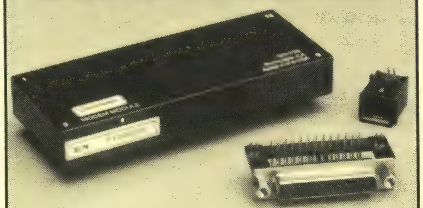

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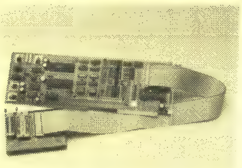

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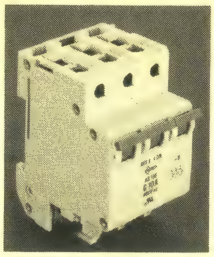

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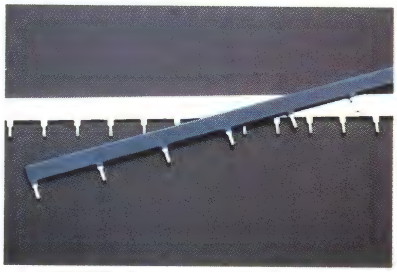

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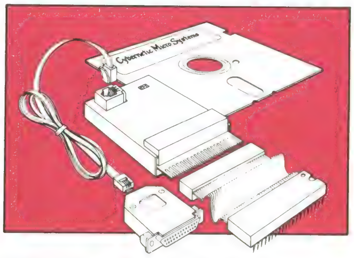

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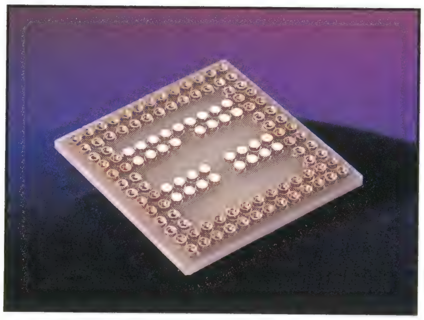

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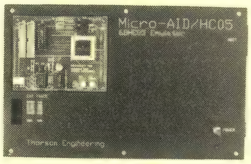

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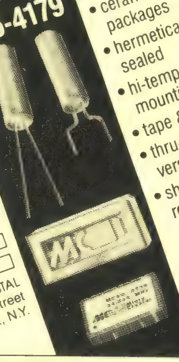

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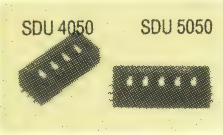

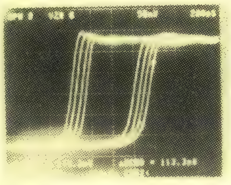

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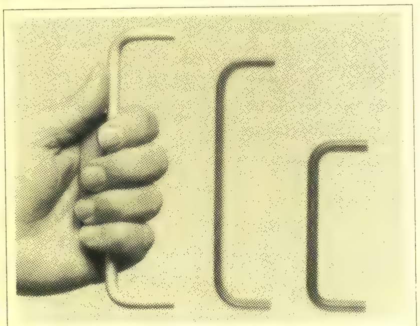

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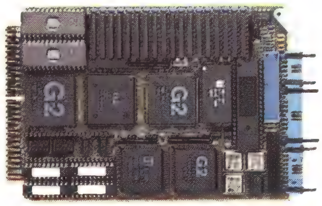

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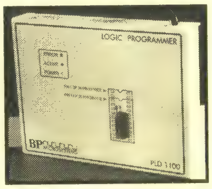

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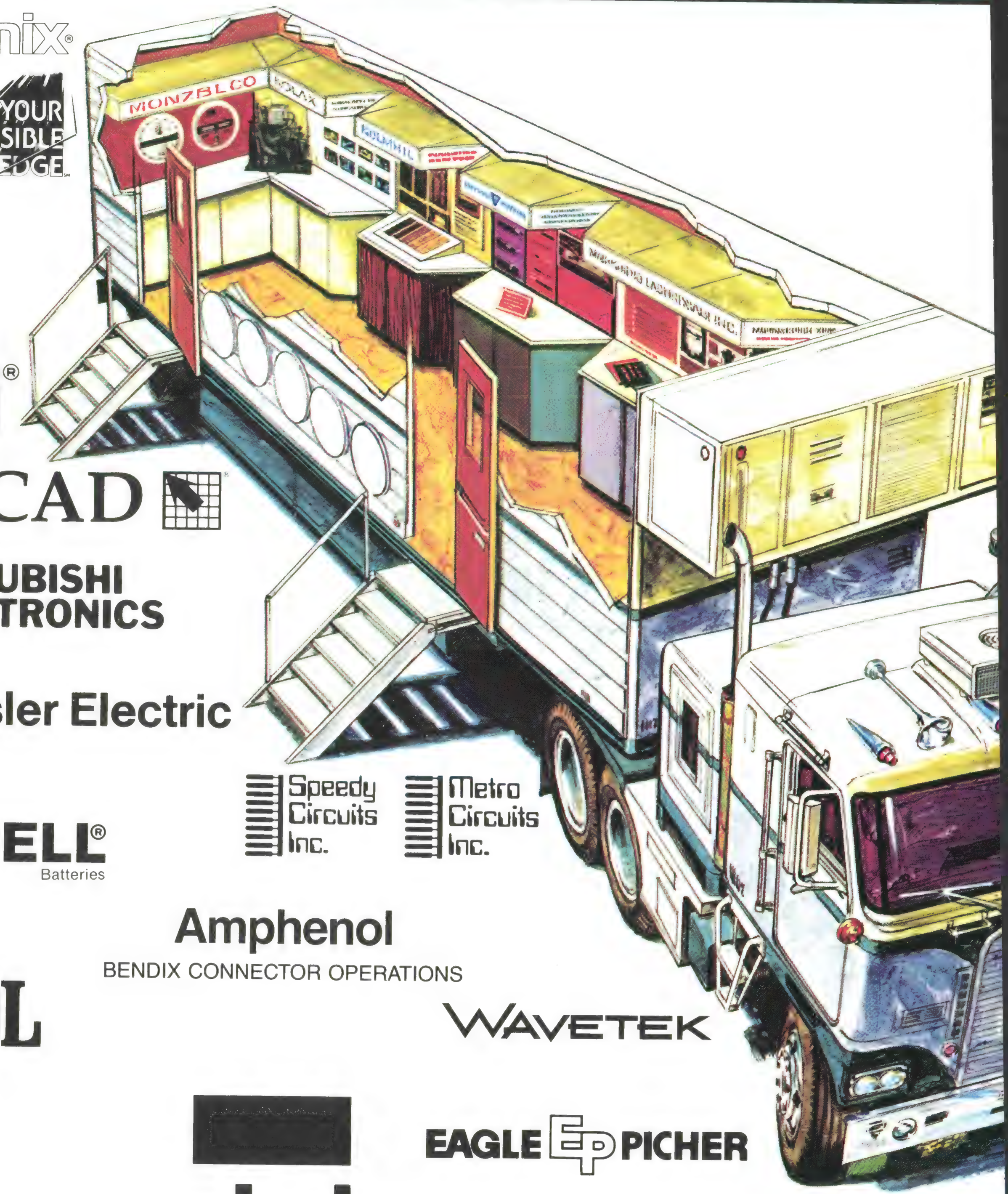

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TENTATIVE SITE ITINERARY
April 2 to May 9 (2nd Half)

DATE	TIME	SITE
April 2 Monday	9:00-11:30 AM	UNISYS CORPORATION Marcus Avenue, Great Neck, NY
April 2 Monday	1:30-3:30 PM	LORAL ELECTRONIC SYSTEMS Ridge Hill, Yonkers, NY
April 3 Tuesday	8:00-10:30 AM	IBM CORPORATION Neighborhood Road, Kingston, NY
April 3 Tuesday	12:00-3:00 PM	IBM CORPORATION South Road, Poughkeepsie, NY
April 4 Wednesday	9:00-11:30 AM	IBM CORPORATION, East Fishkill Route 52, Hopewell Junction, NY
April 4 Wednesday	1:30-4:00 PM	IBM CORPORATION Route 134, Yorktown Heights, NY
April 5 Thursday	8:00-10:00 AM	PITNEY BOWES 380 Main Avenue, Norwalk, CT
April 5 Thursday	11:00-12:30 AM-PM	PERKIN-ELMER CORPORATION 50 Danbury Road, Wilton, CT
April 5 Thursday	2:00-4:00 PM	HUGHES OPTICAL SYSTEMS 100 Wooster Heights Road, Danbury, CT
April 6 Friday	8:30-10:00 AM	PITNEY BOWES One Waterview Drive, Shelton, CT
April 6 Friday	11:30-1:00 AM-PM	GENERAL DATACOMM, INC. Straights Turnpike-Route 63, Middlebury, CT
April 6 Friday	2:00-4:00 PM	DATAPRODUCTS NEW ENGLAND, INC./COROMETRICS MEDICAL 50 Barnes Park North, Wallingford, CT
April 9 Monday	9:00-10:30 AM	RAYTHEON COMPANY, Equipment Division 1001 Boston Post Road, Marlboro, MA
April 9 Monday	11:30-1:00 AM-PM	RAYTHEON COMPANY, Equipment Division 528 Boston Post Road, Sudbury, MA
April 9 Monday	2:30-4:00 PM	RAYTHEON COMPANY, Equipment Division 430 Boston Post Road, Wayland, MA
April 10 Tuesday	9:00-10:30 AM	PRIME COMPUTER, INC. 500 Old Connecticut Path, Framingham, MA
April 10 Tuesday	12:00-3:00 PM	NORTHROP CORPORATION 100 Morse Street, Norwood, MA
April 11 Wednesday	8:30-10:30 AM	THE FOXBORO COMPANY 38 Neponset Avenue, Foxboro, MA
April 11 Wednesday	12:30-3:00 AM-PM	CODEX CORPORATION 5 Dan Road, Canton, MA
April 16 Monday	9:00-11:30 AM	SANDERS ASSOCIATES 95 Canal Street, Nashua, NH
April 16 Monday	2:00-4:00 PM	SANDERS ASSOCIATES Route 3 North, Merrimack, NH
April 17 Tuesday	8:30-10:00 AM	SANDERS ASSOCIATES 63 River Road, Hudson, NH
April 17 Tuesday	12:00-3:00 AM-PM	AT&T TECHNOLOGIES/BELL LABS 1600 Osgood Street, N. Andover, MA
April 18 Wednesday	8:30-11:00 AM	WANG LABORATORIES 1 Industrial Avenue, Lowell, MA
April 18 Wednesday	2:30-4:30 PM	POLAROID CORPORATION 565 Technology Square, Cambridge, MA
April 19 Thursday	8:30-10:30 AM	GENRAD, INC. 300 Baker Street, Concord, MA
April 19 Thursday	11:30-1:30 AM-PM	DIGITAL EQUIPMENT CORPORATION 126 Main Street, Maynard, MA
April 19 Thursday	2:30-4:00 PM	STRATUS COMPUTER INC. 55 Fairbanks Boulevard, Marlboro, MA
April 20 Friday	9:00-11:00 AM	DIGITAL EQUIPMENT CORPORATION 200 Forest Street, Marlboro, MA
April 20 Friday	1:00-3:00 PM	DATA GENERAL CORPORATION 4400 Computer Drive, Westboro, MA
April 23 Monday	9:00-11:00 AM	GENERAL ELECTRIC COMPANY One River Road, Schenectady, NY
April 23 Monday	1:30-4:00 PM	GENERAL ELECTRIC COMPANY Broad Street, Utica, NY
April 24 Tuesday	9:00-11:30 AM	GENERAL ELECTRIC COMPANY French Road, Utica, NY
April 25 Wednesday	9:00-11:30 AM	GENERAL ELECTRIC COMPANY W. Dover, Binghampton, NY
April 25 Wednesday	1:00-3:30 PM	IBM CORPORATION, Glendale Labs Route 17C & Glendale Dr., Endicott, NY
April 26 Thursday	9:00-12:00 AM	IBM CORPORATION, Federal Systems Route 17C, Owego, NY
April 27 Friday	9:00-11:30 AM	XEROX CORPORATION 800 Phillips Road, Henrietta, NY
April 27 Friday	1:00-4:00 PM	EASTMAN KODAK COMPANY 901 Elmgrove Road, Rochester, NY
April 30 Monday	9:00-11:30 AM	ALLEN-BRADLEY COMPANY 747 Alpha Drive, Highland Heights, OH
April 30 Monday	12:30-2:00 PM	PICKER INTERNATIONAL 595 Miner Road, Highland Heights, OH
April 30 Monday	3:00-4:30 PM	KEITHLEY INSTRUMENTS INC. 28775 Aurora Road, Solon, OH
May 1 Tuesday	9:00-11:30 AM	WESTINGHOUSE ELECTRIC CORP., Science & Tech. Ctr. 1310 Beulah Rd., Pittsburgh, PA
May 1 Tuesday	2:00-4:00 PM	NCR CORPORATION 800 Cochran Avenue, Cambridge, OH
May 2 Wednesday	9:00-11:30 AM	AT&T NETWORK SYSTEMS 6200 East Broad Street, Columbus, OH
May 2 Wednesday	2:00-4:30 PM	SYSTEMS RESEARCH LABORATORIES 2000 Indian Ripple Road, Dayton, OH
May 3 Thursday	8:30-11:00 AM	CINCINNATI ELECTRONICS 2630 Glendale-Milford Rd., Cincinnati, OH
May 3 Thursday	11:30-1:00 PM	XETRON CORPORATION 40 W. Crescentville Road, Cincinnati, OH
May 3 Thursday	2:00-4:00 PM	GENERAL ELECTRIC CO., Evendale Plant I 75 & Neuman Way, Cincinnati, OH
May 4 Friday	9:00-11:00 AM	AT&T TECHNOLOGIES, Consumer Products 6612 E. 75th Street, Indianapolis, IN
May 4 Friday	1:00-3:00 PM	THOMSON CONSUMER ELECTRONICS 600 N. Sherman Avenue, Indianapolis, IN
May 7 Monday	9:00-11:00 AM	DELCO ELECTRONICS 1800 E. Lincoln Road, Kokomo, IN
May 7 Monday	2:00-4:00 PM	ITT CORPORATION, Aerospace Optical Div. 1919 West Cook Road, Ft. Wayne, IN
May 8 Tuesday	8:30-11:00 AM	MAGNAVOX GOVERNMENT & INDUSTRIAL ELECTRONICS 1313 Production Road, Ft. Wayne, IN
May 8 Tuesday	2:00-4:00 PM	HEATH/ZENITH DATA SYSTEMS Hilltop Road, St. Joseph, MI
May 9 Wednesday	9:00-11:00 AM	UNISYS CORPORATION 41100 Plymouth Road, Plymouth, MI

Schedule subject to change.

CIRCLE NO. 144

CAREER OPPORTUNITIES

1990 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
News Edition	Apr. 19	Mar. 30	ICs/Graphics Controllers/Microprocessors, Industrial Automation, Regional Profile: So. California
Magazine Edition	Apr. 26	Apr. 5	Computer Boards/Microprocessors, Power Sources, Sensors/Transducers, Special Design Project #4, Electro Show Issue
News Edition	May 3	Apr. 12	CAE/Board Layout, Education, Special Supplement: ASICs, Electro Show Issue
Magazine Edition	May 10	Apr. 19	Analogy Technology Special Issue—Analog ICs, Analog Instruments, Digital ICs/ Microprocessors/ASICs, Special Design Project #5
News Edition	May 17	Apr. 27	ICs/Memory ICs, Test & Measurement, Regional Profile: Massachusetts & New Hampshire
Magazine Edition	May 24	May 3	Microprocessors, Computers & Peripherals, Semicustom ICs/ASICs, Components, Sensors & Transducers
Magazine Edition	June 7	May 17	Software, Design Tools, Microprocessor I/O Chips, μP Support Chip Directory
News Edition	June 14	May 24	Peripherals/Input Devices, Software, Special Supplement: EDA

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ELECTRICAL/COMPUTER: Analog and RF circuit design, receiver or transmitter RF circuits; LCD display technology, acoustics, and 8-bit microprocessor software; infrared and fiber optics; low speed data; digital modulation; 900 Mhz RF power amplifier design with hybrid or microstrip circuitry; RF device development with device vendors; parallel and/or push-pull RF amplifier design at 900 Mhz or UHF; A/D and D/A convertors; RF propagation; passive and active filter theory; microwave antenna design; UL, EMI and RFI requirements; HP 3062 test system; HP 9000; digital hardware, microprocessor applications and interfaces; digital switching technology; firmware development methodology; PCM and digital telephony; digital signal processing; ASIC design; LAN systems, PSTN standards, ISDN standards, processor architectures, high-speed logic; 16-bit MPU design practices, programmable logic; digital modulation synchronization, adaptive signal processing, viterbi algorithm and MLSE, decision Feedback equalizer; convolutional code and linear block code; speech coding, echo cancellation, encryption; CAE techniques for digital hardware design using Mentor Graphics, etc.; data communications protocols (CCITT #7, OSI, X.25, X.75, PAD, LAPB, LAPD, Ethernet, ISDN, CCITT V series modem, group 3 fax); computer network management/administration (Apollo, Sun, Mentor Graphics, AppleTalk). BSEE/MSEE/ BSCE/BSCS or equivalent. Respond to Dept. EC.

MECHANICAL: Electronic packaging; CAD, CV CADDS 4X; materials selection and geometric tolerances and dimensioning; extruded metal; injection molded plastics; life test procedures and factory introduction and support; plating materials and processes; structural analysis modeling; die casting and sheet metal stampings; thermal management. BSME/ MSME or equivalent. Respond to Dept. ME.

SYSTEMS: Radio/cellular communication systems engineering; RF propagation prediction methods; PSTN traffic planning; telephone network, interconnection and telecommunication industry standards; microwave system design and equipment engineering; telephone switching systems; software programming skills. BSEE/BSCE/ BSCS or equivalent. Respond to Dept. S.

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Individual will have a minimum of 7 years experience managing Software Engineers in an MS-DOS or UNIX environment. Must have demonstrated ability to utilize computer based project tracking, management and productivity tools. Applicants should have expertise with "C" language, micro-computer development, and the ability to manage market-driven, crucial projects. Dept. DED.

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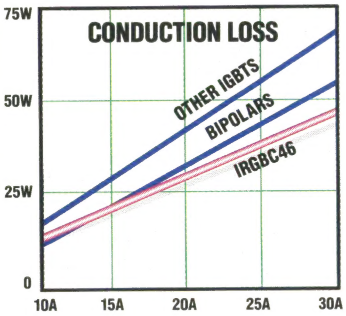

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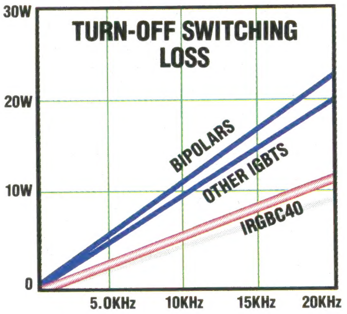

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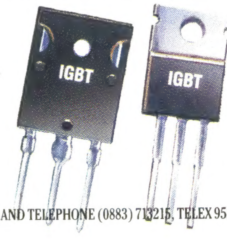

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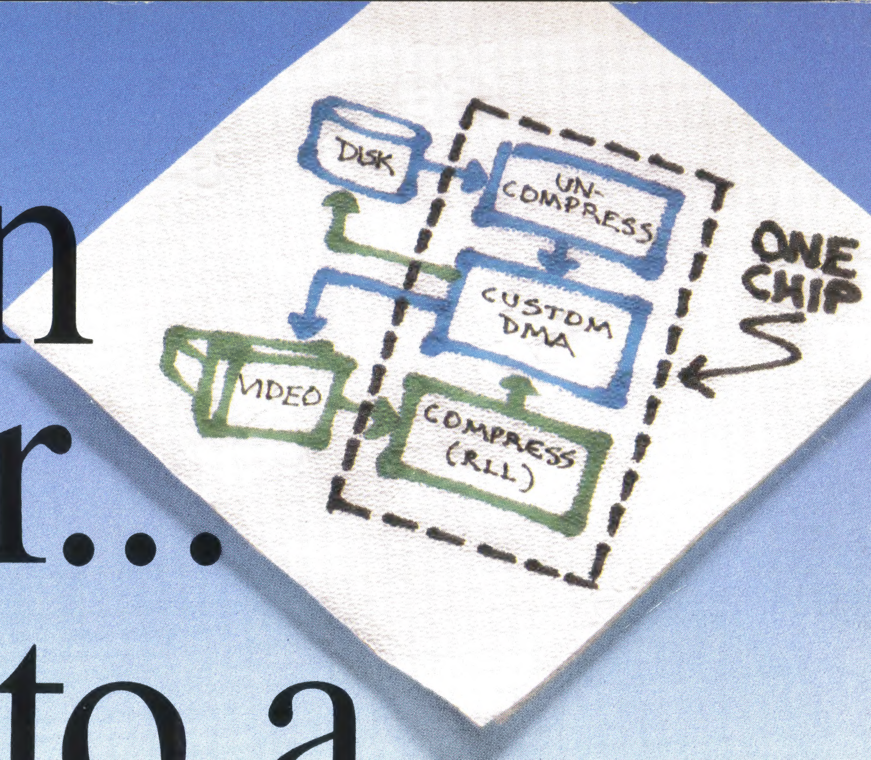

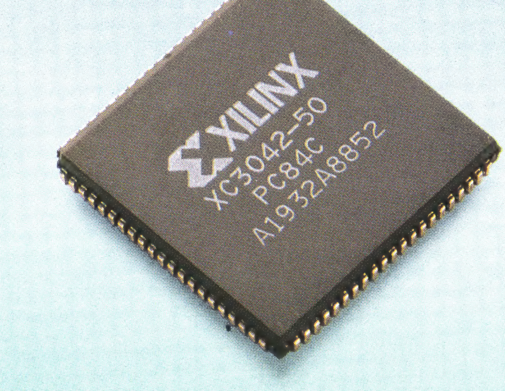

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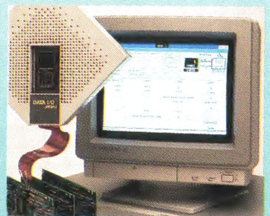

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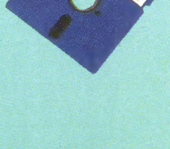

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